

SILIGURI INSTITUTE OF TECHNOLOGY
Department of Electronics & Communication Engineering

Name of the Paper: <i>Analog Electronics</i>	Paper code: <i>ECF391</i>
Name of the student: <i>Srujan Chakraborty</i>	Branch: <i>ECE</i> Roll no: <i>12</i>

Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)					Marks	Total marks	Signature of teacher with date
<i>02</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>20</i>	<i>87</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>22</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>8</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>20</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>8</i>		
Date: <i>27/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		

<i>03</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>20</i>	<i>89</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>23</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>20</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
Date: <i>28/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>6</i>		

<i>01</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>20</i>	<i>90</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>23</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>20</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
Date: <i>18/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		

<i>04</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>19</i>	<i>86</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>22</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>16</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
Date: <i>17/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>6</i>		

<i>06</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>21</i>	<i>91</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>23</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>20</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
Date: <i>14/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		

<i>07</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		<i>20</i>	<i>85</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		<i>22</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>9</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		<i>18</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>8</i>		
Date: <i>21/08/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		<i>8</i>		

SILIGURI INSTITUTE OF TECHNOLOGY
Department of Electronics & Communication Engineering

Name of the Paper: <i>Analog Electronics Circuit</i>	Paper code: <i>EC-391</i>
Name of the student: <i>Sneha Chakraborty</i> Branch: <i>EEF</i>	Roll no: <i>11900317014</i>

Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)				Marks	Total marks	Signature of teacher with date
Experiment no: <i>05</i>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	<i>20</i>	<i>84</i>	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	<i>22</i>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<i>8</i>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	<i>18</i>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<i>7</i>		
Date: <i>20/11/18</i>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<i>9</i>		

name of the Paper: <u>Analog Electronic Circuit</u>	Paper code: <u>EC-391</u>
name of the student: <u>Debanjona Bhattacharya</u> Branch: <u>ECE</u>	Roll no: <u>40</u>

Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)					Marks	Total marks	Signature of teacher with date
Experiment no: 1	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		24	95	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		24		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		20		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		

Experiment no: 2	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		24	89	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		20		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		

Experiment no: 3	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		23	88	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		22		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		17		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		

Experiment no: 4	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		24	90	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		24		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		8		

Experiment no: 5	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		24	93	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		24		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		

Experiment no: 6	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		24	94	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		24		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		19		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		9		

EXPERIMENT-4

AIM :

To design and implement a voltage to current converter using Op-amp 741.

OBJECTIVE :

The purpose of this experiment is to design and implement a voltage to current converter using Op-amp 741 and study its linear characteristics.

APPARATUS & COMPONENTS REQUIRED :

Sl. No.	Name of Apparatus or Components	Specification	Maker's Name	Quantity
1.	IC	Op-amp 741	—	1
2.	Resistors	10k Ω , 1k Ω , 100 Ω	—	5
3.	DMM	(0-20)V	CIE	1
4.	Micro Ammeter	(0-10)mA	COSMO	1
5.	DC power supply	(0-10)V, $\pm$ 15V	ELNOVA	1
6.	Breadboard	—	—	1
7.	Connecting wires	—	—	as per required.

CIRCUIT DIAGRAM :

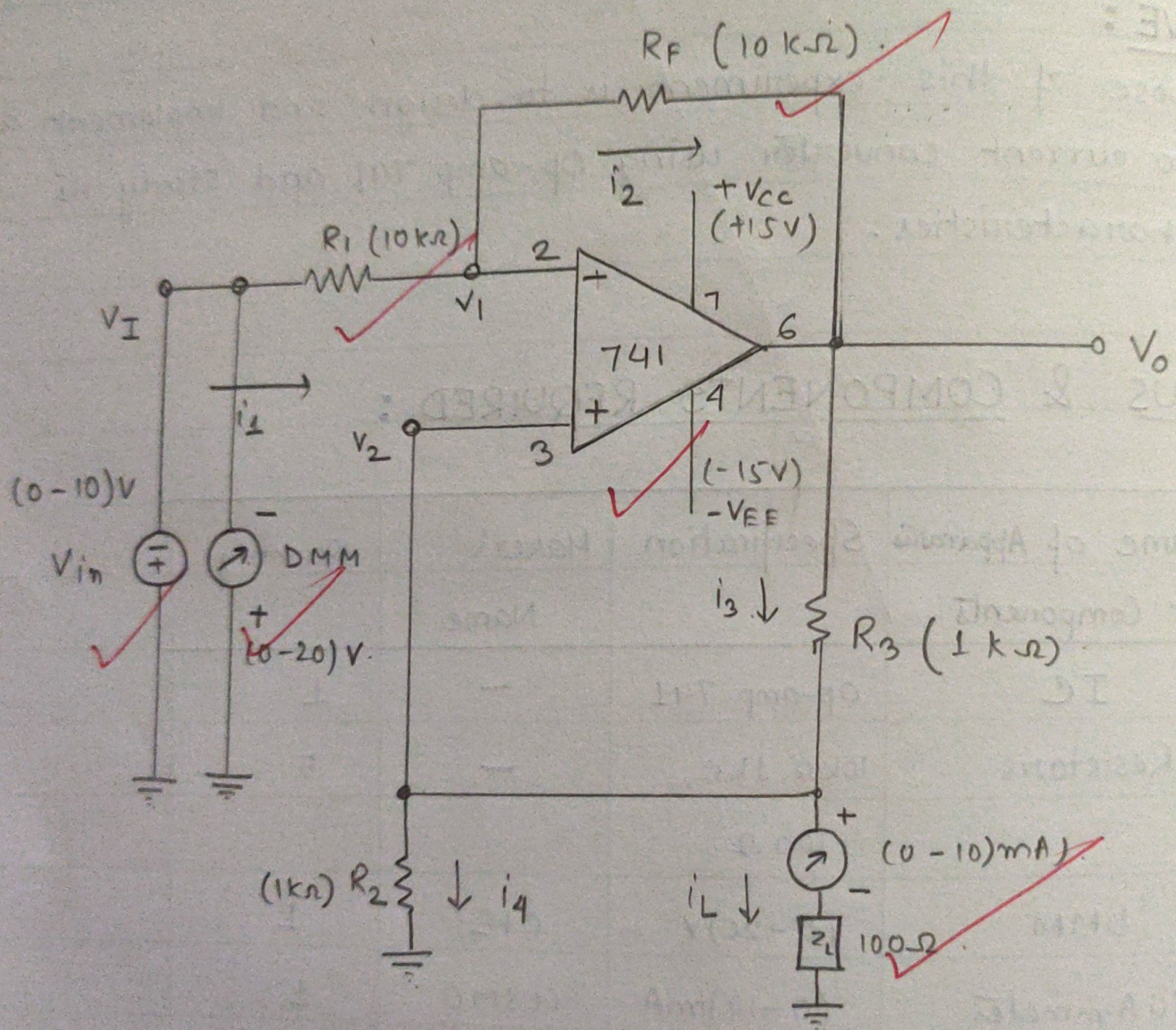


Fig: 1(a). Voltage to Current Converter using Op-Amp 741

THEORY:

The very high forward gain and differential input nature of the operational amplifier can be used to create a nearly ideal voltage controlled current source or V to I converter. The input voltage to be converted is applied to the non-inverting terminal of the op-amp. The inverting input terminal is connected in feedback to one end of resistor and the source of transistor.

From the fig: 1(a) —

$$V_1 = 0, \quad V_2 = 0.$$

Because of virtual ground concept, V_1 is the virtual ground.

$$i_1 = i_2, \quad i_1 = \frac{V_I}{R_I} = i_2$$

$$\text{So } i_2 = \frac{V_I}{R_I} \text{ or } i_2 \propto V_I.$$

Here, i_2 is independent of R_F .

To find $i_L \propto V_I$ independent of Z_L .

Virtual short concept:

$$V_1 = V_2 = V_I - i_L Z_L.$$

$$i_1 = i_2.$$

$$\Rightarrow \frac{V_I - i_L Z_L}{R_I} = \frac{i_L Z_L - V_O}{R_F} \quad \text{--- (1)}$$

$$\frac{V_O - i_L Z_L}{R_F} = \frac{i_L Z_L - V_I}{R_I}$$

$$\Rightarrow V_O - i_L Z_L = \frac{R_F (i_L Z_L - V_I)}{R_I}$$

Summing up the currents at V_L node.

$$i_3 = i_4 + i_L$$

$$\Rightarrow \frac{V_0 - i_L Z_L}{R_3} = i_L + \frac{i_L Z_L}{R_2}$$

$$\therefore \frac{R_F}{R_1} \cdot i_L Z_L - \frac{R_F}{R_1 R_3} V_I = i_L + \frac{i_L Z_L}{R_2}$$

$$\Rightarrow \frac{R_F}{R_1 R_3} i_L Z_L - i_L - \frac{i_L Z_L}{R_2} = \frac{R_F}{R_1 R_3} V_I$$

$$\Rightarrow i_L \left\{ Z_L \left(\frac{R_F}{R_1 R_3} - \frac{1}{R_2} \right) - 1 \right\} = \frac{R_F}{R_1 R_3} V_I$$

To keep i_L independent of Z_L we should have coefficient of Z_L as zero —

$$\text{So } \frac{R_F}{R_1 R_3} - \frac{1}{R_2} = 0$$

$$\boxed{\frac{1}{R_2} = \frac{R_F}{R_1 R_3}}$$

$$i_L = -V_I \left(\frac{R_F}{R_1 R_3} \right)$$

$$i_L = -V_I \left(\frac{1}{R_2} \right)$$

The designed V-I converter will be functional till the output voltage is within the limit.

DESIGN PROBLEM

Q. An input voltage varying from (0-10)V drives a voltage to current converter to produce an output current $i_L = (0-10)\text{mA}$. Find out the value of R_2, R_3 . Given value of $R_1 = 10\text{k}\Omega$ and $R_F = 10\text{k}\Omega$.

$$\rightarrow \text{Condition} - \frac{1}{R_2} = \frac{R_F}{R_1 R_3}$$

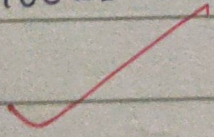
$$i_L = -V_I \left(\frac{1}{R_2} \right)$$

$$\Rightarrow 10 \times 10^{-3} = 10 \left(\frac{1}{R_2} \right)$$

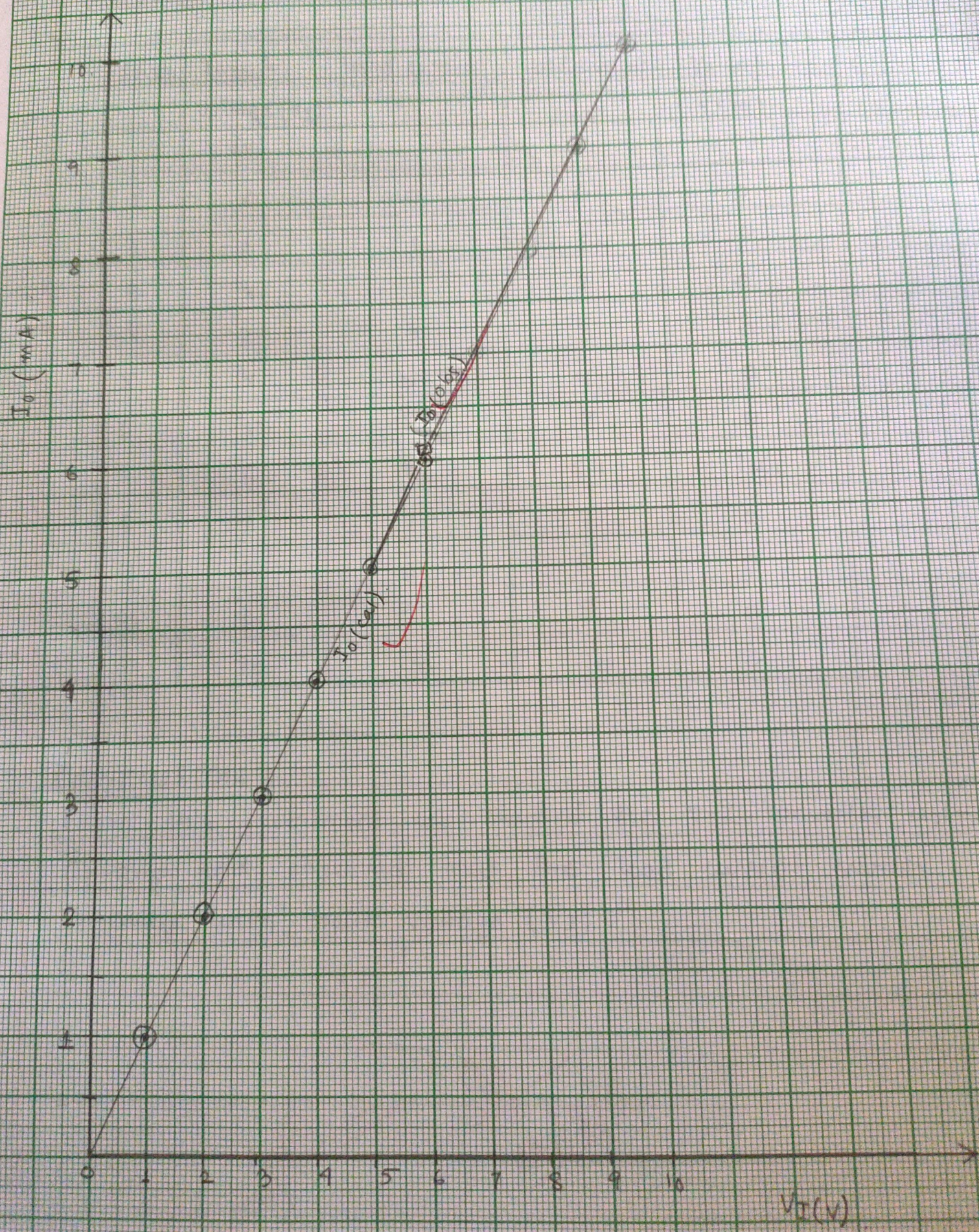
$$\Rightarrow R_2 = 1\text{k}\Omega$$

$$\text{Also, } 1 = \frac{10}{10 \times R_3}$$

$$R_3 = 1\text{k}\Omega$$

$$\text{Choose } Z_L = 100\Omega$$


SCALE:
X AXIS: 1 cm = 1 V
Y AXIS: 1 cm = 1 mA



OBSERVATION TABLE :

Sl. No.	Input voltage (V_I) (v)	Load current (I_L) cal. (mA)	Load current (obs.) (I_L) (mA)	% of error.
1	0	0	0	0
2	1	1	1	0
3	2	2	2	0
4	3	3	3	0
5	4	4	4	0
6	5	5	5	0
7	6	6	6.1	1.66
8	7	7	7	0
9	8	8	8	0
10	9	9	9	0
11	10	10	10	0

CONCLUSION :

From this experiment, we studied the V-I converter using Op-amp and observed that the load current varies linearly with Input voltage (V_I).

EXPERIMENT-7AIM :

To design and implement an Astable multivibrator using NE555.

OBJECTIVE :

The purpose of this experiment is to construct

- i) a rectangular wave generating circuit.
- ii) a clock source using NE555.

APPARATUS/COMPONENTS REQUIRED :

SL. No.	NAME	SPECIFICATION	MAKER	QUANTITY
1.	IC	NE555	—	1
2.	Breadboard	—	—	1
3.	Resistor	1k Ω , 6.8k Ω	—	2
4.	Capacitor	0.01 μ F, 0.1 μ F	—	2
5.	DC power supply	5V	ELNOVA	1
6.	CRO	30MHz	GWINSTEK	1
7.	BNC crocodile probe	—	—	1
8.	Connecting wires	—	—	As per reqd.
9.	DMM	—	CIE	1

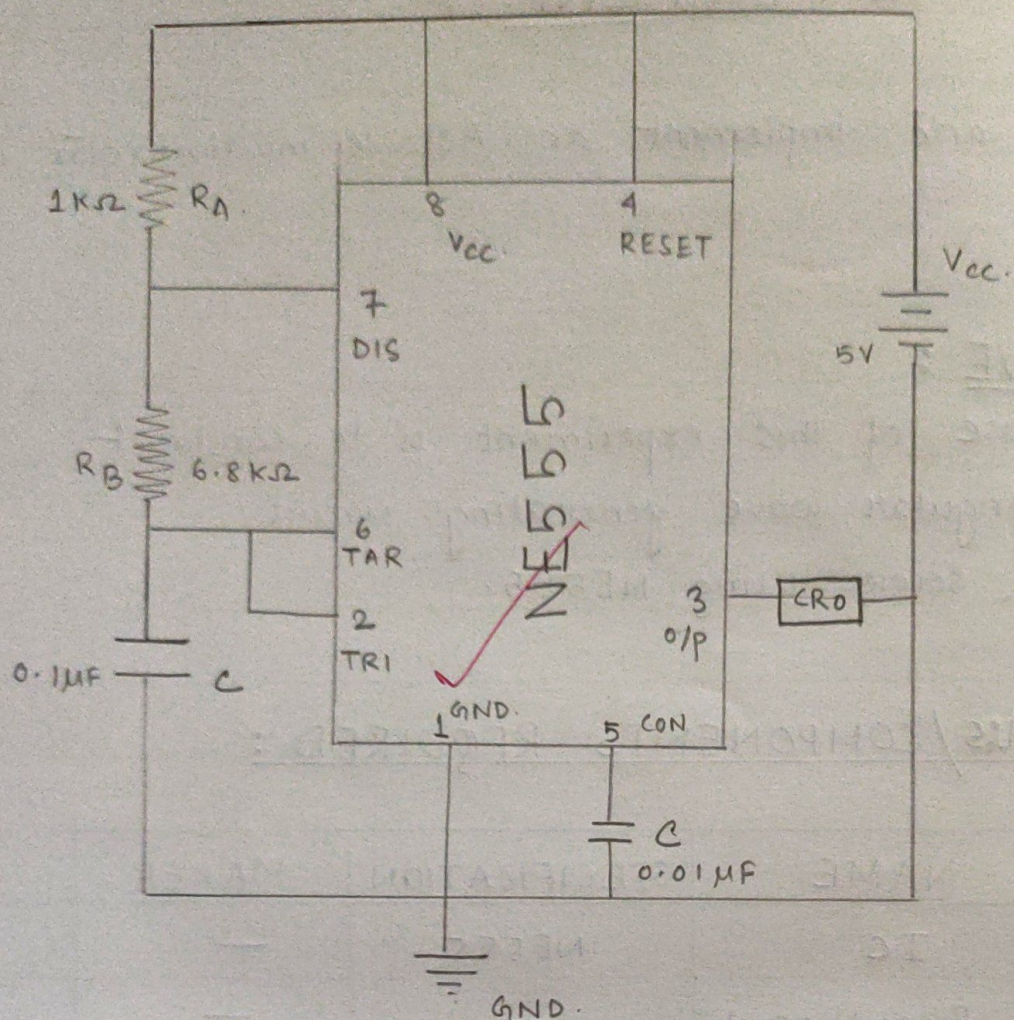
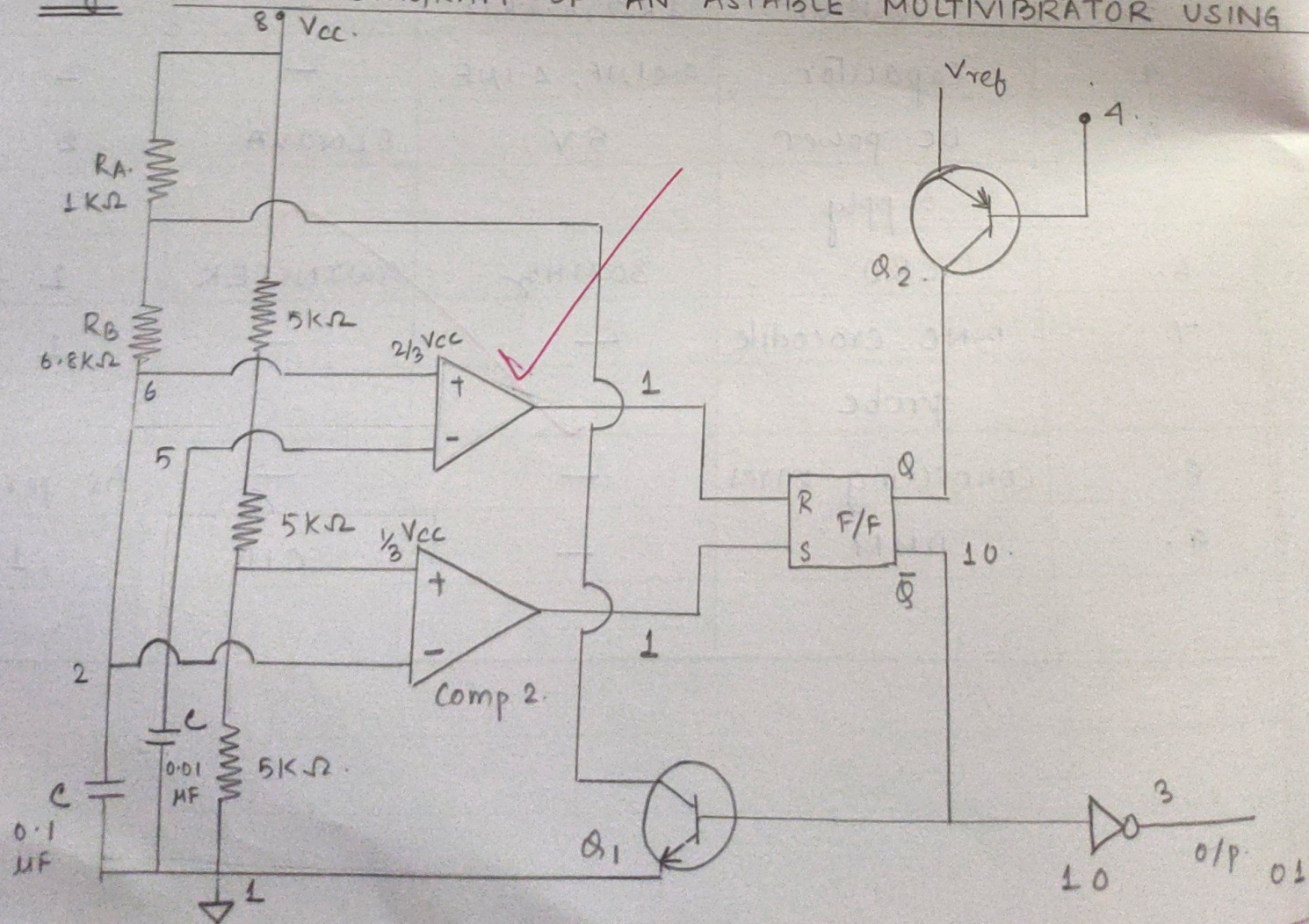


Fig: CIRCUIT DIAGRAM OF AN ASTABLE MULTIVIBRATOR USING N



THEORY :

Astable Multivibrator mode of 555 timer of IC is also called Free running or self-triggering mode. Unlike Monostable Multivibrator mode it doesn't have any stable state, it has two quasi stable states (HIGH and LOW). No external triggering is required in Astable mode, it automatically interchange its two states on a particular interval, hence generates a rectangular waveform. The time duration of HIGH and LOW output is determined by the external resistances and a capacitor. Astable mode acts as an oscillator circuit, in which output oscillates at a particular frequency and generates pulses in rectangular waveform.

In Astable multivibrator —

$$t_c = 0.69 (R_A + R_B) C.$$

$$t_d = 0.69 R_B C.$$

$$T = t_c + t_d = 0.69 (R_A + 2R_B) C.$$

$$f_0 = \frac{1}{T} = \frac{1}{0.69 (R_A + 2R_B) C}$$

$$f_0 = \frac{1.45}{(R_A + 2R_B) C}.$$

$$\% \text{ of Duty cycle} = \frac{T_c}{T} = \frac{0.69 (R_A + R_B) \times C}{0.69 (R_A + 2R_B) C}$$

$$= \frac{R_A + R_B}{R_A + 2R_B} \times 100.$$

Teacher's Signature

DESIGN PROBLEM:

Q. Design an astable multivibrator using NE555 to produce 1 kHz rectangular wave. $[R_A = 1k\Omega, C = 0.1\mu F]$.
Find R_B and % of duty cycle.

$$\rightarrow 1 \times 10^3 = \frac{1.45}{(1 \times 10^3 + 2R_B) \times 0.1 \times 10^{-6}}$$

$$\Rightarrow 1 \times 10^3 \times 0.1 \times 10^{-6} = \frac{1.45}{(1 \times 10^3 + 2R_B)}$$

$$\Rightarrow 2R_B + 10^3 = \frac{1.45}{10^3 \times 0.1 \times 10^{-6}}$$

$$\Rightarrow 2R_B + 10^3 = 14500 \quad \Rightarrow 2R_B = 1350.$$

$$\Rightarrow R_B = 6.75 k\Omega.$$

Here we use nearest standard value (6.8 k Ω).

$$\begin{aligned} \% \text{ of Duty cycle} &= \frac{1 + 6.8}{1 + 2 \times 6.8} \times 100 \\ &= 53.42 \% \end{aligned}$$

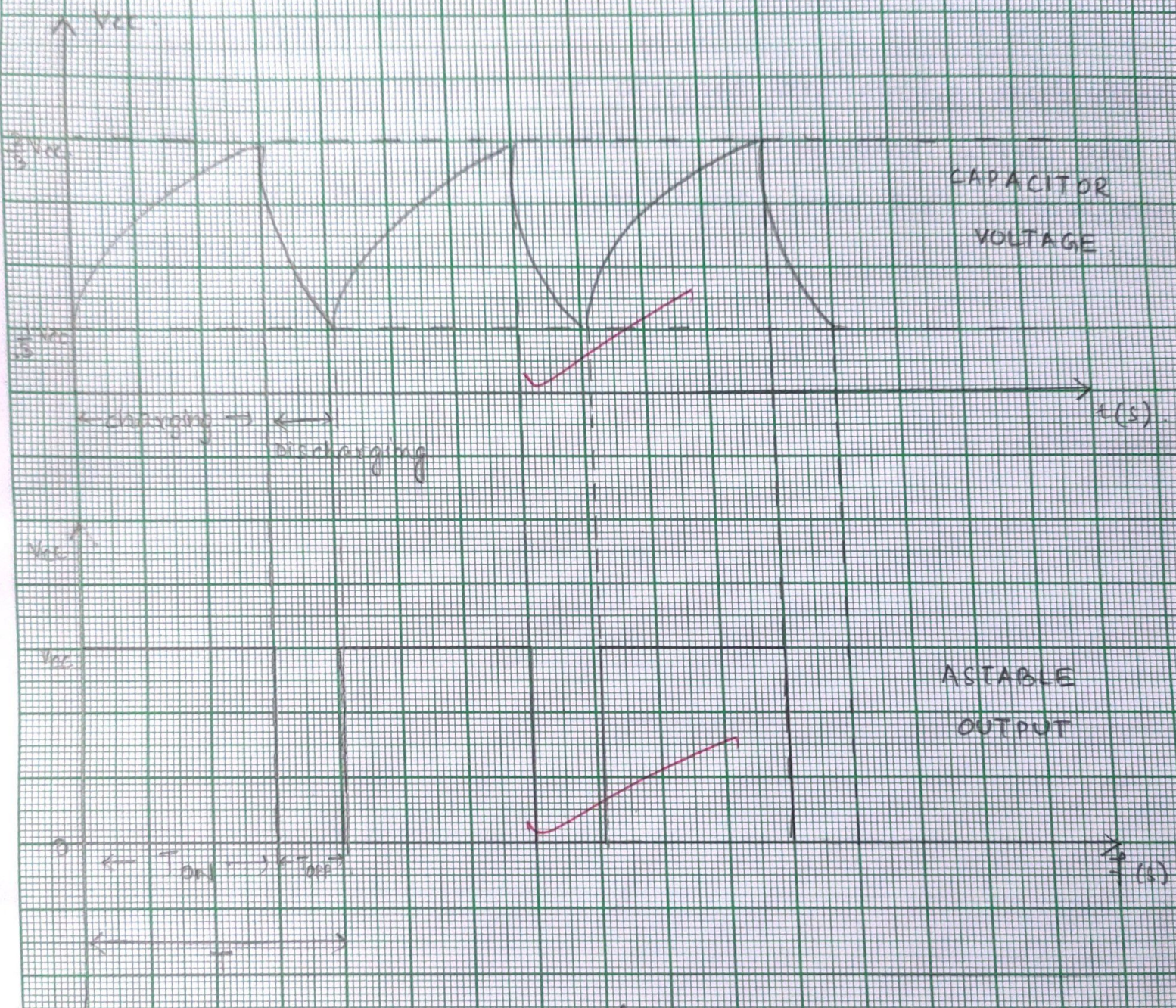


Fig: Output waveform of an Astable Multivibrator

OBSERVATION TABLE :

R_A (K Ω)	R_B (K Ω)	C (μ F)	T_{ON} (s)	T_{OFF} (s)	f_o (cal) (KHz)	f_o (obs) = $\frac{1}{T}$ (KHz)	% of ERROR	% OF DUTY CYCLE	% OF DUTY CYCLE = $\frac{T_{ON}}{T} \times 100$ (obs)
			(2.7 $\times$ 0.2) ms	(2.5 $\times$ 0.2) ms					
1	6.8	0.1	= 0.54 ms	= 0.5 ms	1	0.96	4%	53.4	51.92
			= 0.54×10^{-3} s	0.005 s					

CONCLUSION :

From this experiment we designed an astable multivibrator using NE555 and generated a rectangular wave and calculated the % of duty cycle from the observations obtained.

~~29/11/18~~

as voltage

Aim: To study Zener Diode, Regulator.

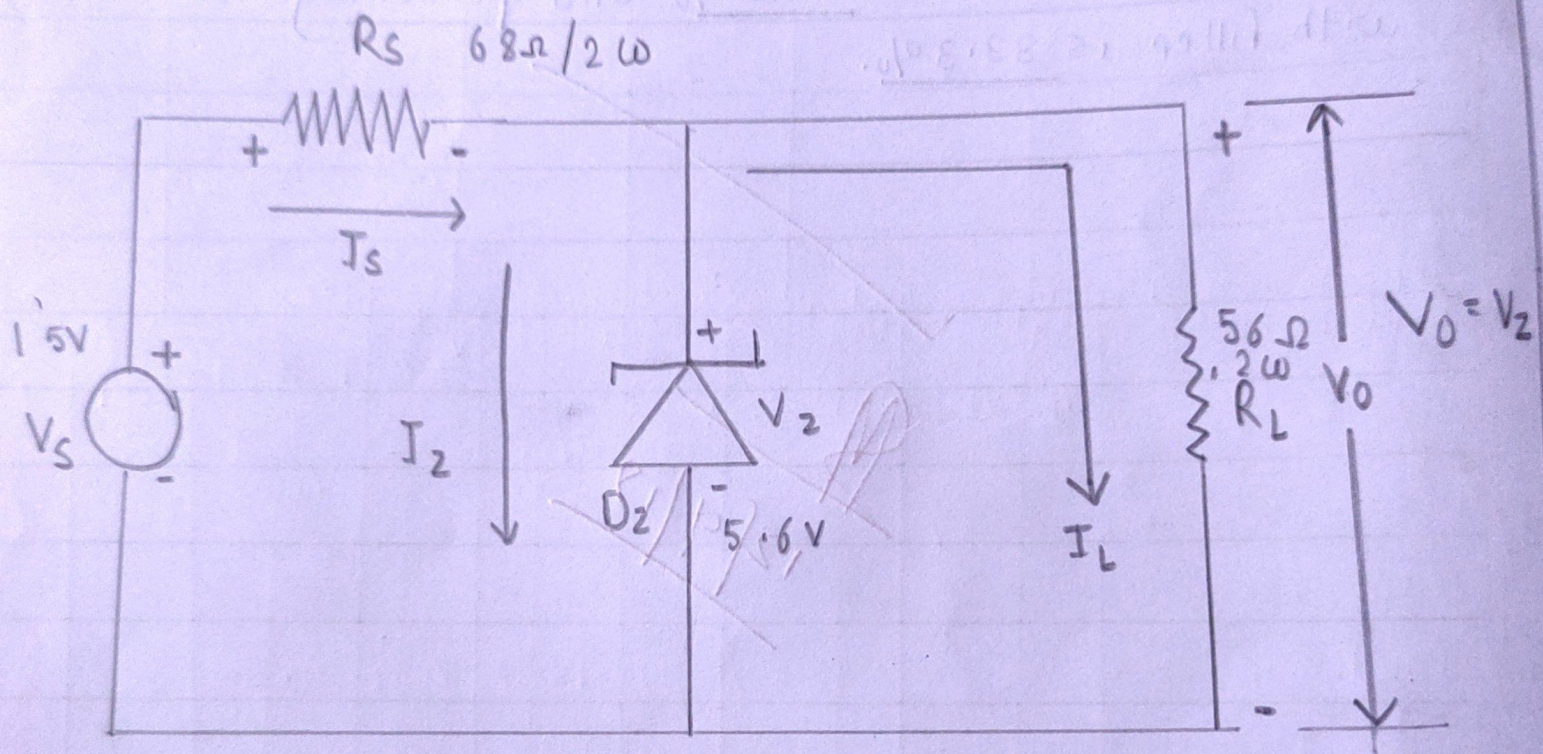
OBJECTIVE: (1) To study Zener Diode as voltage regulator, when the input voltage (V_s) is variable while the load resistance (R_L) is fixed.

- (2) To study the Zener diode Regulator when the input voltage (V_s) is fixed while the load resistance (R_L) is variable.
- (3) To calculate the percentage of source regulation.
- (4) To calculate the percentage of load regulation.

~~Theory~~

APPARATUS REQUIRED:

S.No	NAME OF THE APPARATUS	SPECIFICATION	MAKER'S NAME	QUANTITY
1.	Zener Diode	1N4734A (5.6V, 1W)		1
2.	DC Unregulated Power Supply	(0-30) V	ELMOVA	1
3.	D.M.M (Digital Voltmeter)	(0-20) V	CIE 122	1
4.	Resistors	$R_s = 68\Omega (2W)$ $R_L = 33\Omega, 47\Omega,$ $56\Omega, 82\Omega, 390\Omega,$ $1K\Omega, 10K\Omega, 36K\Omega$ $82K\Omega, 200K\Omega,$ $470K\Omega (1W)$		12
5.	Breadboard	—		1
6.	Connecting Wires	—	—	As required



CIRCUIT DIAGRAM OF ZENER DIODE AS
 VOLTAGE REGULATOR

$$V_{RS} = V_S - V_Z$$

$$V_S > V_Z$$

THEORY:

Zener diode is a P-N junction diode specially designed to operate in the reverse biased mode. It has a particular voltage known as breakdown voltage, at which the diode breaks down while reverse biased.

The basic principle of Zener diode is the Zener breakdown. When a diode is heavily doped, its depletion region will be narrow. When a high reverse voltage is applied across the junction, there will be very strong electric field at the junction.

The input source current, $I_s = I_z + I_L$ — (1)

The drop across the series resistance is $R_s = V_{in} - V_z$ — (2)

And the current through it, $I_s = (V_{in} - V_z) / R_s$ — (3)

from (1) and (2), we get,

$$(V_{in} - V_z) / R_s = I_z + I_L \text{ — (4)}$$

Regulation with varying input voltage (line regulation):

It is defined as the change in the regulated ~~voltage~~ voltage with respect to variation in line voltage.

In this, input voltage varies but load resistance remains constant hence the load current remains constant. The output voltage remains constant. If there is a decrease in V_{in} , I_z decreases as load current remains constant and voltage drop across R_s is reduced. But even though I_z may change, V_z remains constant keeping V_o constant.

- Regulation with the varying load (load regulation)
It is defined as change in load voltage with respect to variations in load current. The input voltage is constant and output voltage varies due to change in the load resistance value.

Considering output voltage is increased due to increase in load current, $(V_{in} - V_z)/R_s$ is constant. Then, as load current changes, the Zener Diode I_z will also change but in opposite way such that the sum of I_z and I_L will remain constant.

Design a Zener diode voltage regulator to provide 5.6V regulated supply at maximum load current 110mA and minimum load current 0 with $(15V \pm 10\%)$ input unregulated DC source. Select diode of proper rating $\{I_{zmax}, V_z, I_{zmin}, \text{Power Dissipation and } R_L\}$.

→ Given, $V_z = 5.6V = V_o$, $I_{Lmax} = 110mA$, $I_{Lmin} = 0mA$

$$V_{smax} = 15 \pm 0.1 \times 15 = 16.5V$$

$$V_{smin} = 15 - 0.1 \times 15 = 13.5V$$

$$I_{zmax} = \frac{V_{smax} - V_z}{R_s} - \frac{V_{zmax}}{R_L}$$

$$\text{Now, } R_s = \left(\frac{V_{smax} - V_z}{I_{zmax} + I_{Lmin}} \right) \quad \& \quad R_s = \left(\frac{V_{smin} - V_z}{0.01 I_{zmax} + I_{Lmax}} \right)$$

$$\frac{V_{smax} - V_z}{I_{zmax} + I_{Lmin}} = \frac{V_{smin} - V_z}{0.01 I_{zmax} + I_{Lmax}}$$

$$\Rightarrow \frac{16.5 - 5.6}{I_{zmax} + 0} = \frac{13.5 - 5.6}{0.01 I_{zmax} + 110}$$

$$\Rightarrow 7.9 I_{zmax} = 0.109 I_{zmax} + 1.199$$

$$\Rightarrow 7.791 I_{zmax} = 1.199$$

$$\Rightarrow I_{zmax} = 154 \text{ mA}$$

$$I_{zmin} = \frac{154}{0.01} \text{ mA} = 1.54 \text{ mA}$$

$$P_{DZ} = V_z \times I_{zmax} = 5.6 \times 154 \text{ W} = 0.86 \text{ W}$$

$$R_s = \frac{16.5 - 5.6}{154} = \frac{10.9}{154 \times 10^{-3}} = 70.8 \Omega$$

$$R_L = \frac{V_o}{I_{Lmax}} = \frac{5.6 \times 10^3}{110} \Omega = 50.9 \Omega$$

1N4734A is the diode of proper rating
 $I_{ZT} = 45 \text{ mA}$, $I_{zmax} = 162 \text{ mA}$, $I_{zmin} = 1 \text{ mA}$ [nearest standard values]

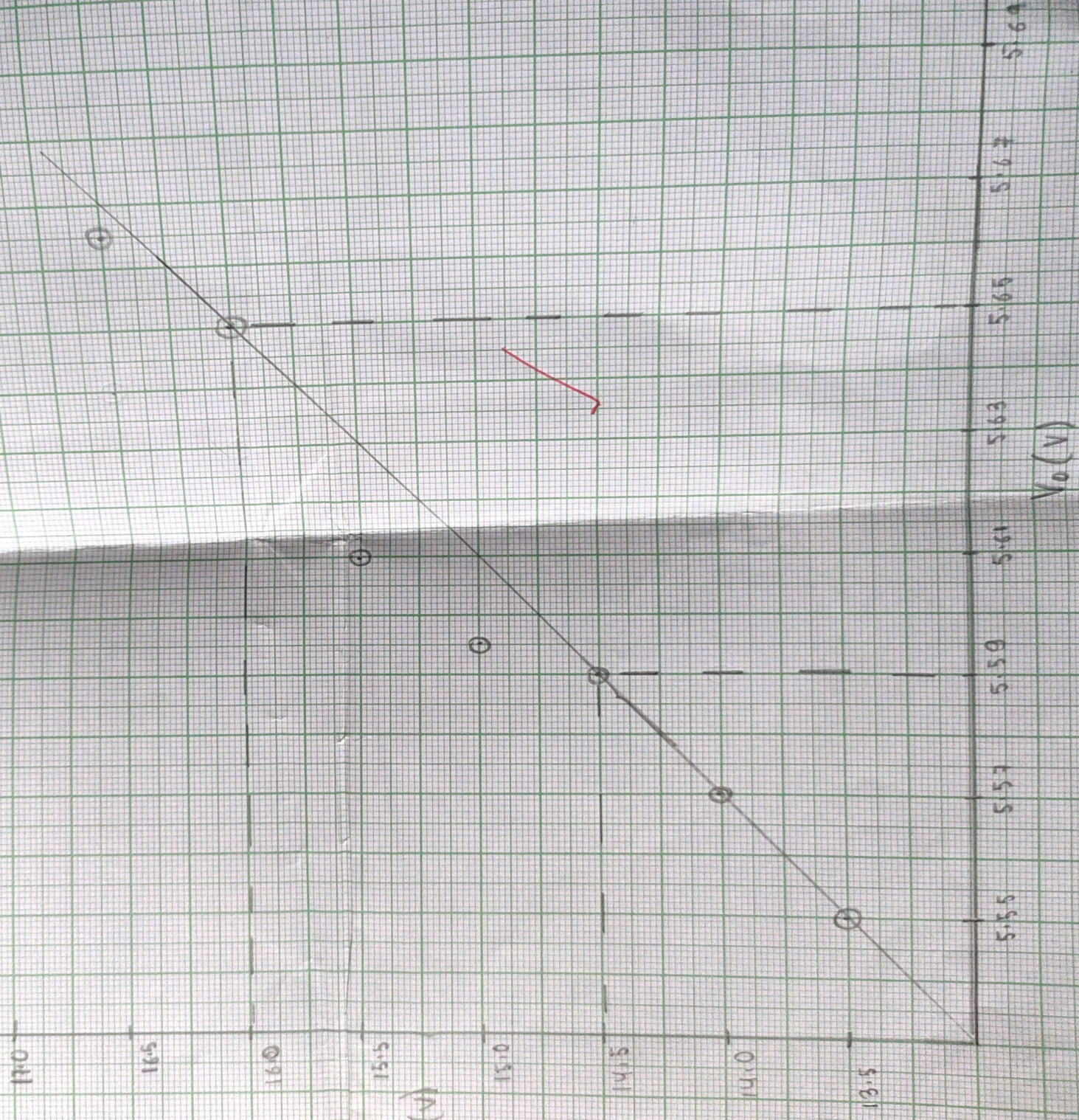
$$P_{DZ} = 1 \text{ W}$$

$$R_s = \frac{\Delta V_z}{\Delta I_s} = 5 \Omega$$

$$R_s = 68 \Omega \text{ (nearest standard value), } 2 \text{ W}$$

$$\frac{V_{R_s}^2}{R_s} = \frac{(16.5 - 5.6)^2}{68} = 1.75 \text{ W, we use } 2 \text{ W.}$$

Scale: y-axis = 0.025V
 x-axis = 0.001V



$$I_{Lmax} = \frac{5.6}{47} = 119 \text{ mA}$$

$$P_D \text{ of } R_L = 119^2 \times 47 \text{ W} = 0.62 \text{ W}$$

Choose $R_L = 47 \Omega$, 1 W

Observation table:-

I. SOURCE REGULATION:

Sl. No	$V_S(V)$	$R_L(\Omega)$	$V_O(V)$	% of source regulation = $\frac{\Delta V_O \text{ for } \pm 10\% \text{ change in } V_S}{V_O} \times 100\%$
1	13.5		5.55	
2	14.0		5.57	$= \frac{5.6 - 5.5}{5.5} \times 100\%$
3	14.5	56 Ω	5.59	
4	15.0		5.595	$= 1.81\%$
5	15.5		5.61	
6	16.0		5.65	
7	16.5		5.66	

II. LOAD REGULATION:

Sl. No	$V_S(V)$	$R_L(\Omega)$	$V_O(V)$	% of load regulation = $\frac{V_{O1} - V_{O2}}{V_{O1}} \times 100\%$
1		33	4.9	
2		47	5.5	
3	15	56	5.5	$= \frac{5.7 - 5.5}{5.5} \times 100\%$
4		82	5.6	
5		390	5.6	$= 3.63\%$
6		1 k Ω	5.6	
7		10 k Ω	5.6	
8		36 k Ω	5.6	

Teacher's Signature.....

Sl. No	$R_L(\Omega)$	$V_o(V)$	$V_s(V)$	% of load regulation
9	82k Ω	5.6		
10	200k Ω	5.7	15V	
11	470k Ω	5.7		
12	Open	5.7		

CONCLUSION:

Voltage Regulation experiment was successfully performed. The value of percentage of source regulation is 1.81% and the value of percentage of load regulation is 3.63%.

~~25/9/18~~

rpt.No. 03

Characteristics of PN junction diode :

- Aim : To study V-I characteristics of a P-N junction diode.
- Objective : To study and plot V-I characteristics of a PN junction diode and determine the following parameters.

1. Cut-in voltage.
2. static forward resistance, R_{ac}

where,

$$R_{ac} = \frac{V_D}{I_D} (\Omega)$$

3. Dynamic forward resistance R_{ac}

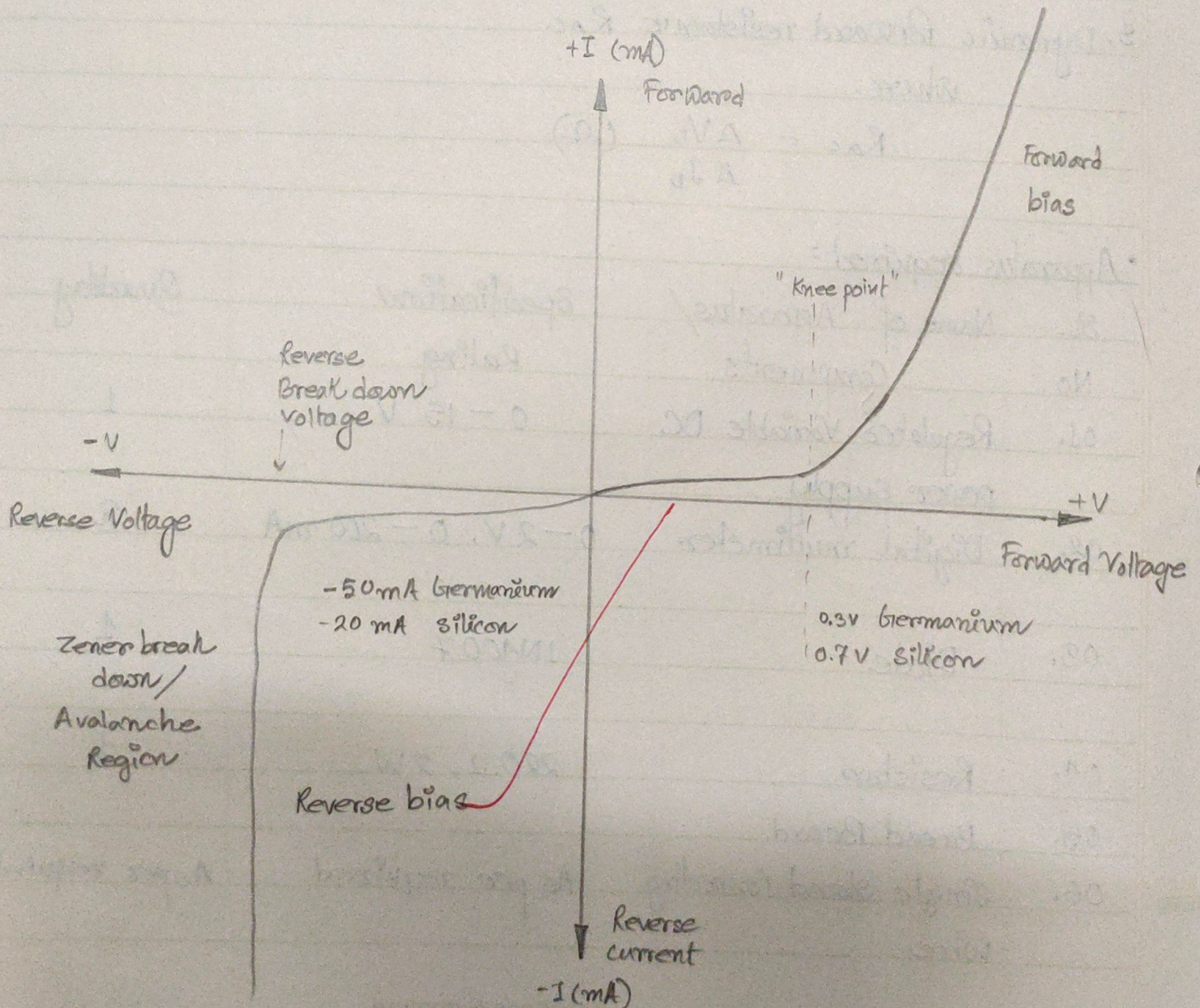
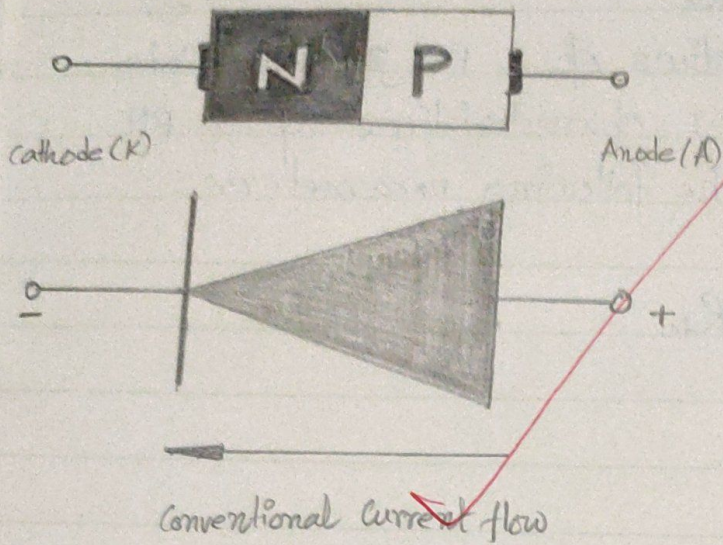
where

$$R_{ac} = \frac{\Delta V_D}{\Delta I_D} (\Omega)$$

• Apparatus required :

Sl No.	Name of Apparatus/ Components	Specification/ Rating	Quantity
01.	Regulated Variable DC power supply	0 - 15 V	1
02.	Digital multimeter	0 - 2 V, 0 - 200 mA	2
03.	Diode	1N4007	1
04.	Resistor	220 Ω , 2W	1
05.	Bread Board.		
06.	Single strand Connecting wire	As per required	As per required

Junction diode Symbol and static I-V characteristics



• Theory: A P-N junction diode is formed when a p-type semiconductor is fused to an n-type semiconductor creating a potential barrier voltage across the diode junction.

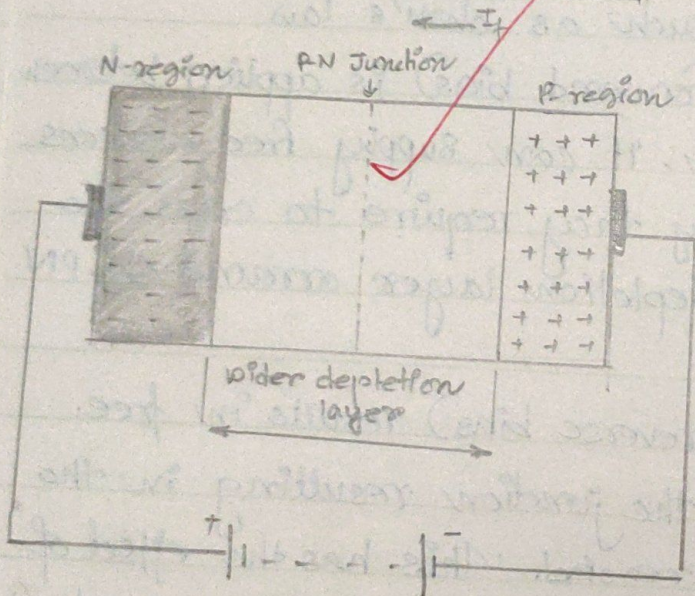
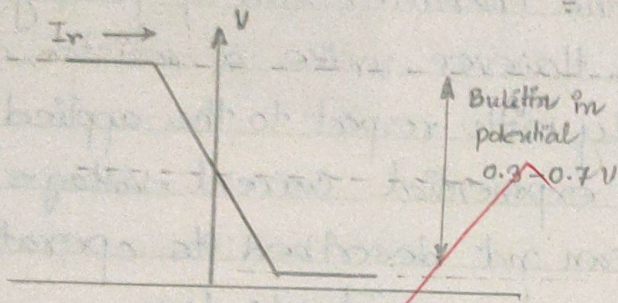
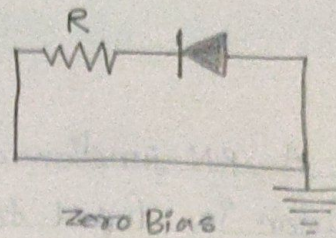
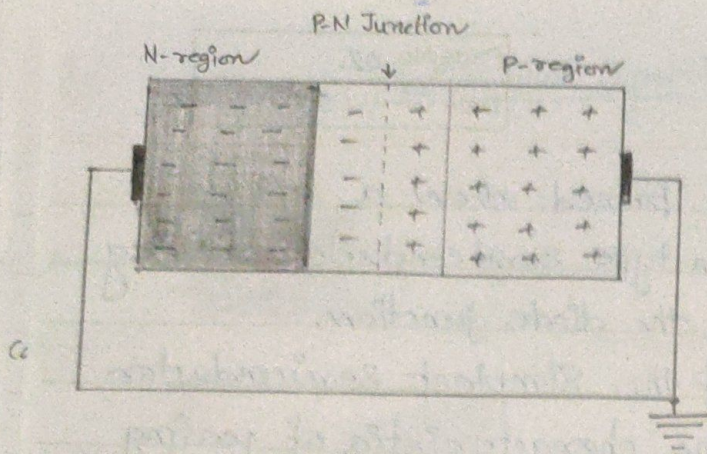
A P-N junction diode is one of the simplest semiconductor device around, and which has the characteristic of passing current in only direction only. However, unlike a resistor, a diode does not behave linearly with respect to the applied voltage as the diode has an exponential current-voltage (I-V) relationship and therefore we can not describe its operation by simply using an equation such as ohm's law.

If a suitable positive voltage (forward bias) is applied between the two ends of the PN junction, it can supply free electrons and holes with the extra energy they require to cross the junction as the width of the depletion layer around the PN junction is decreased.

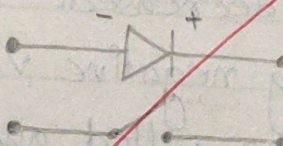
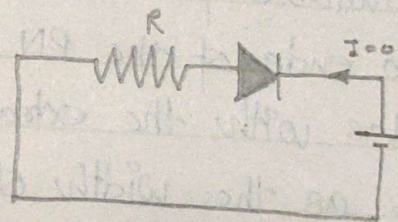
By applying negative voltage (reverse bias) results in free charges being pulled away from the junction resulting in the depletion layer width being increased. This has the effect of increasing or decreasing the effective resistance of the junction itself allowing or blocking current flow through the diode.

There are two operating regions and three possible "biasing" condition for the standard junction Diode and these are:

1. Zero Bias,
2. Reverse Bias,
3. Forward Bias.



Zero Bias P-N junction Diode



Reverse Bias P-N junction Diode

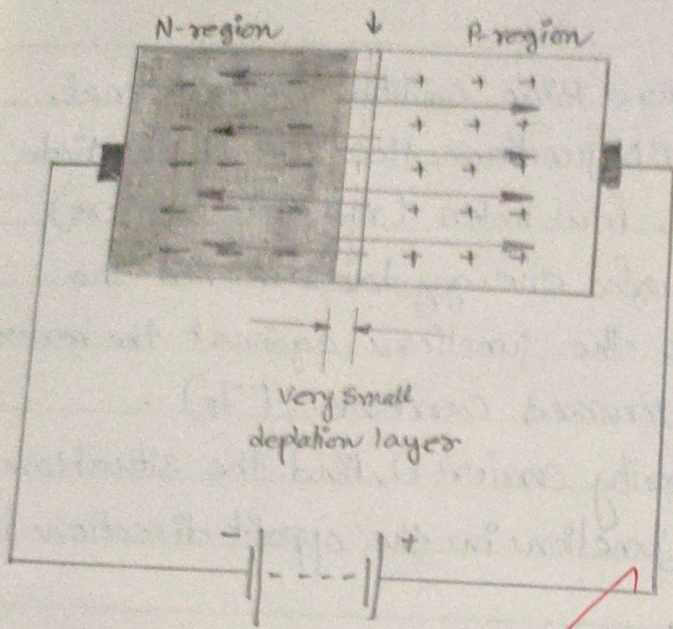
pt. No. 08

Zero Biased PN junction Diode :

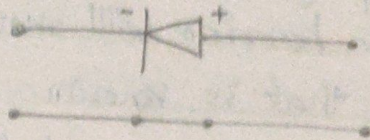
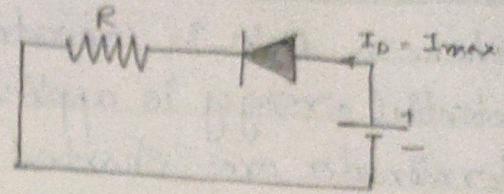
When a diode is connected in a Zero Bias condition, no external potential energy is applied to the PN junction. However if the diode terminals are shorted together, few holes (majority carriers) in the p-type material with enough energy to overcome the potential barrier will move across the junction against the barrier potential that is known as the forward current (I_F). And in N-type material (minority carriers), and the situation favorable and move across the junction in the opposite direction is known as Reverse current (I_R).

Reverse Biased P-N junction Diode : When a diode is connected in a Reverse Bias condition, a positive voltage is applied to the N-type material and a negative voltage is applied to the p-type material. The positive voltage applied to the N-type material, and negative to the p-type material. So N type material attracts electrons toward the positive electrode away from the junction, while the holes in the p-type end are also attracted away from the junction toward the negative electrode. The net result the depletion layer grows wider due to lack of electrons and holes and presents a high impedance path, almost an insulator.

PN junction



Forward Biasing
Voltage



Forward Bias PN junction
Diode

Forward bias PN junction Diode: When a diode is connected in a forward bias condition, a negative voltage is applied to N type material and positive voltage is applied to P type material. If the external voltage becomes greater than the value of potential barrier, approx 0.7 volts for Silicon and 0.3 volts for Germanium, the potential barrier's opposition will be overcome and current will start to flow.

Cut-in Voltage: It is that voltage which is required in forward biased PN junction diode required to overcome the barrier potential.

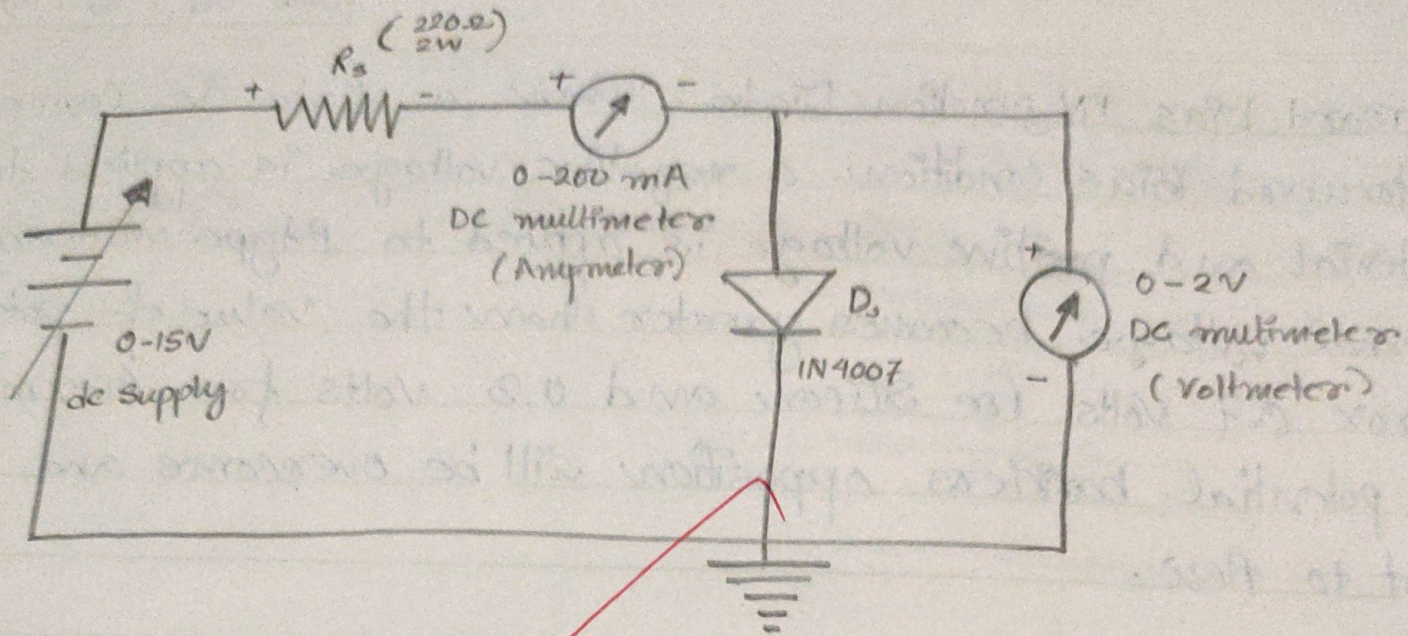
Expression of static forward resistance

$$R_{ac} = \frac{V_D}{I_D} \quad (1)$$

Expression of dynamic forward resistance

$$r_{ac} = \frac{\Delta V_D}{\Delta I_D} \quad (2)$$

The circuit diagram of the given experiment-



$$I_F (\text{max}) = 1 \text{ A}$$

$$V_{R_s} = 1000 \Omega$$

$$R_{ac} = \frac{V_o}{I_o}$$

In x axis one smallest distance = $\frac{0.1}{20} = 0.005$

In y axis one smallest division = $\frac{10}{30} = 0.33 \text{ mA}$

Static Resistance (R_D) = $\frac{V_D}{I_D}$
 $= \frac{0.9 \text{ V}}{20 \times 10^{-3}} = 35.75 \Omega$

Dynamic Resistance (r_D) = $\frac{\Delta V_D}{\Delta I_D} = \frac{0.01}{10.41 \times 10^{-3}} = 0.937 \Omega$

I_D (mA)

(mA)

0.1

0.2

0.3

0.4

0.5

0.6

0.7

0.8

0.9

V_D (Volts) →

Expt. No. 03

• Observation table of V_0 vs I_p

V_0 (Volts)	I_p (mA)
0	0
0.1	0
0.2	0
0.3	0
0.4	0.4
0.5	2.2
0.6	2.9
0.61	3.4
0.62	4.5
0.63	5.0
0.64	6.1
0.65	7.3
0.66	9.0
0.67	11.0
0.68	13.6
0.69	16.6
0.7	20.6
0.71	25.4
0.72	31.3
0.73	37.8
0.74	46.8
0.75	57.3
0.76	69.2

• Calculation:

So, the static resistance,

$$R_{dc} = \frac{V_D}{I_D} = \frac{0.715}{20 \times 10^{-3}} = 35.75 \Omega \text{ (as per graphical value)}$$

And the Dynamic resistance,

$$r_D = \frac{\Delta V_D}{\Delta I_D} = \frac{0.01}{10.67 \times 10^{-3}} = 0.937 \Omega \text{ (as per graphical value)}$$

Cut-in Voltage = 0.715 V - (as per graph)

• Conclusion: After this experiment we understand the characteristics of the P-N junction diode, and the biasing methods. And also we know about the static and dynamic resistance and how it will be calculated.

Teacher's Signature.....

EXPERIMENT - 6

Aim:- To study characteristics curve of a BJT in a common emitter mode.

Objective:- To study and draw the input & output characteristic curve of a Transistor (NPN) in common emitter mode and to calculate the transistor parameters.

- i) Forward current gain $h_{fe} = \Delta I_C / \Delta I_B$ when V_{CE} is const.
- ii) Output admittance $h_{oe} = \Delta I_C / \Delta V_{CE}$ when I_B is const.
- iii) Reverse voltage gain $h_{re} = \Delta V_{BE} / \Delta V_{CE}$ when I_B is const.
- iv) Input Impedance $h_{ie} = \Delta V_{BE} / \Delta I_B$ when V_{CE} is const.

Apparatus and Components used:-

SL No.	Name of Apparatus / Component	Specification / Rating	Quantity	Maker's name.
1.	Regulated DC power supply.	(0-15V)	1	ELNOVA
2.	Digital Multimeter • Digital voltmeter	(0-2V) & (2-20V)	2	CIE
3.	Ammeter	(0-15mA),	1	

$I_B (\mu A)$

$V_{CE} = 0V$

$V_{CE} = 1V$

$I_B = 15 \mu A$
(constant)

$V_{BE} (V)$

$V_{BE} (V)$

Reverse voltage gain, $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$ [I_B is const.]

$I_B (\mu A)$

$V_{CE} = 0V$

$V_{CE} = 1V$

$\Delta I_B (\mu A)$

Input Impedance $h_{ie} = \Delta V_{BE} / \Delta I_B$ when V_{CE} is const.

Fig: Input characteristics curve of a BJT

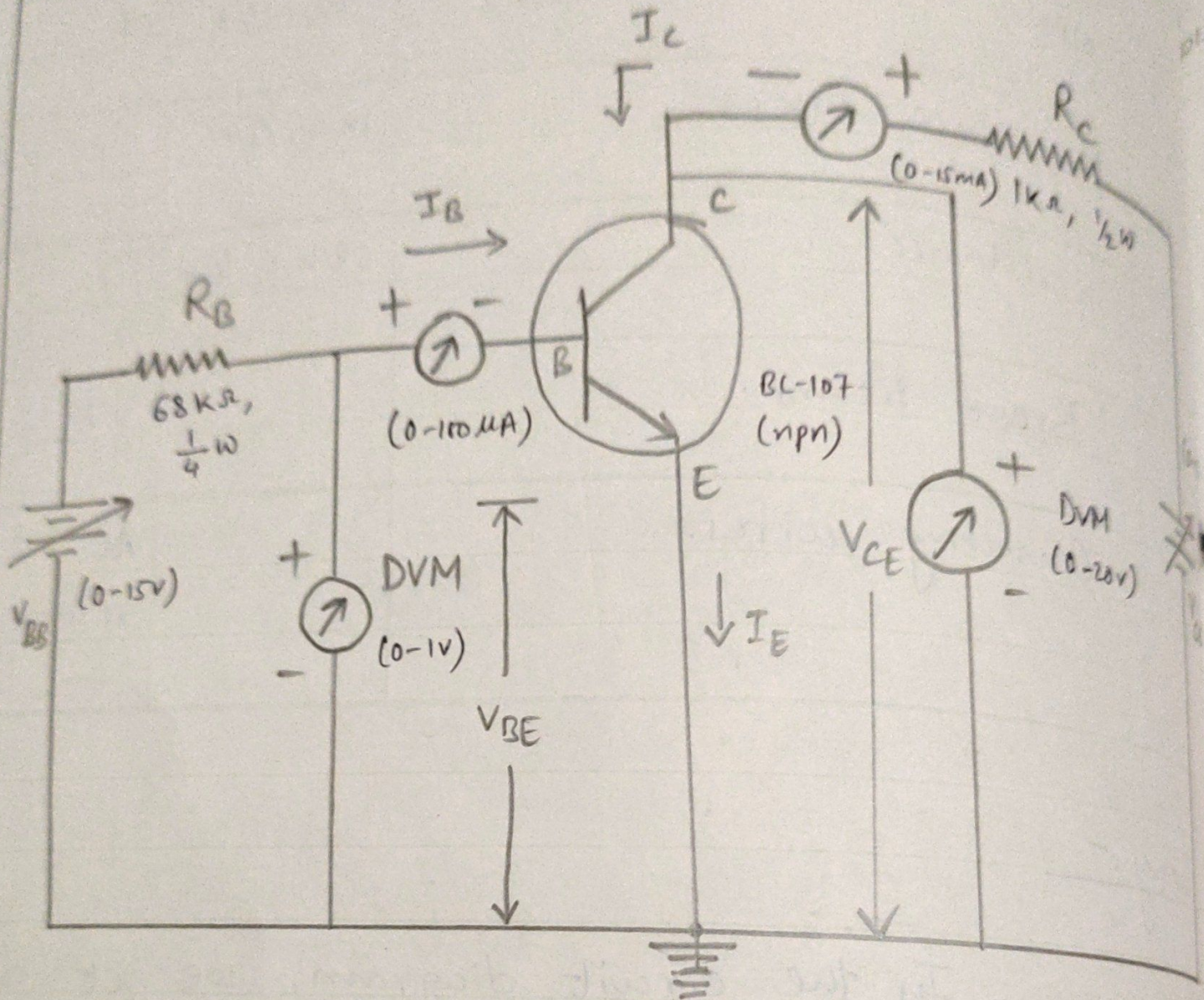
		(0-100 μ A)		
4.	NPN Transistor (BC-107)	BC-107	1	
5.	Resistance (1k Ω)	1k Ω , $\frac{1}{2}$ W	1	
6.	Resistance.	68k Ω , $\frac{1}{4}$ W	1	
7.	Bread Board.		1	
8.	Connecting wires.		As required	

Theory:-

Base curve:- In the circuit diagram, we get data for graphing I_B versus V_{BE} (This is called the input characteristic curve of a BJT in a CE mode). There is nothing surprising here. Since the base-emitter section of a transistor is a diode, we expect to see something resembling a diode curve. There is a fine point worth mentioning, however. As the collector depletion layer widens with increasing collector voltage the base current decreases slightly because of the collector depletion layer captures a few more base electrons. For

Circuit Diagram:-

(Input characteristic)



DVM :- Digital Volt meter.

this reason, if we plot another base curve for different collector voltage the new curve will look slightly different from the old one.

The h parameters Forward current gain ($h_{fe} = \Delta I_C / \Delta I_B$, when V_{CE} is const.), Output Admittance ($h_{oe} = \Delta I_C / \Delta V_{CE}$, when I_B is const.), Reverse voltage gain' ($h_{re} = \Delta V_{BE} / \Delta V_{CE}$, when I_B is const.) and Input Impedance ($h_{ie} = \Delta V_{BE} / \Delta I_B$, when V_{CE} is const.) of the BJT in CE mode can be calculated by the input & output characteristic curves of a BJT in CE mode.

Observation Table:-

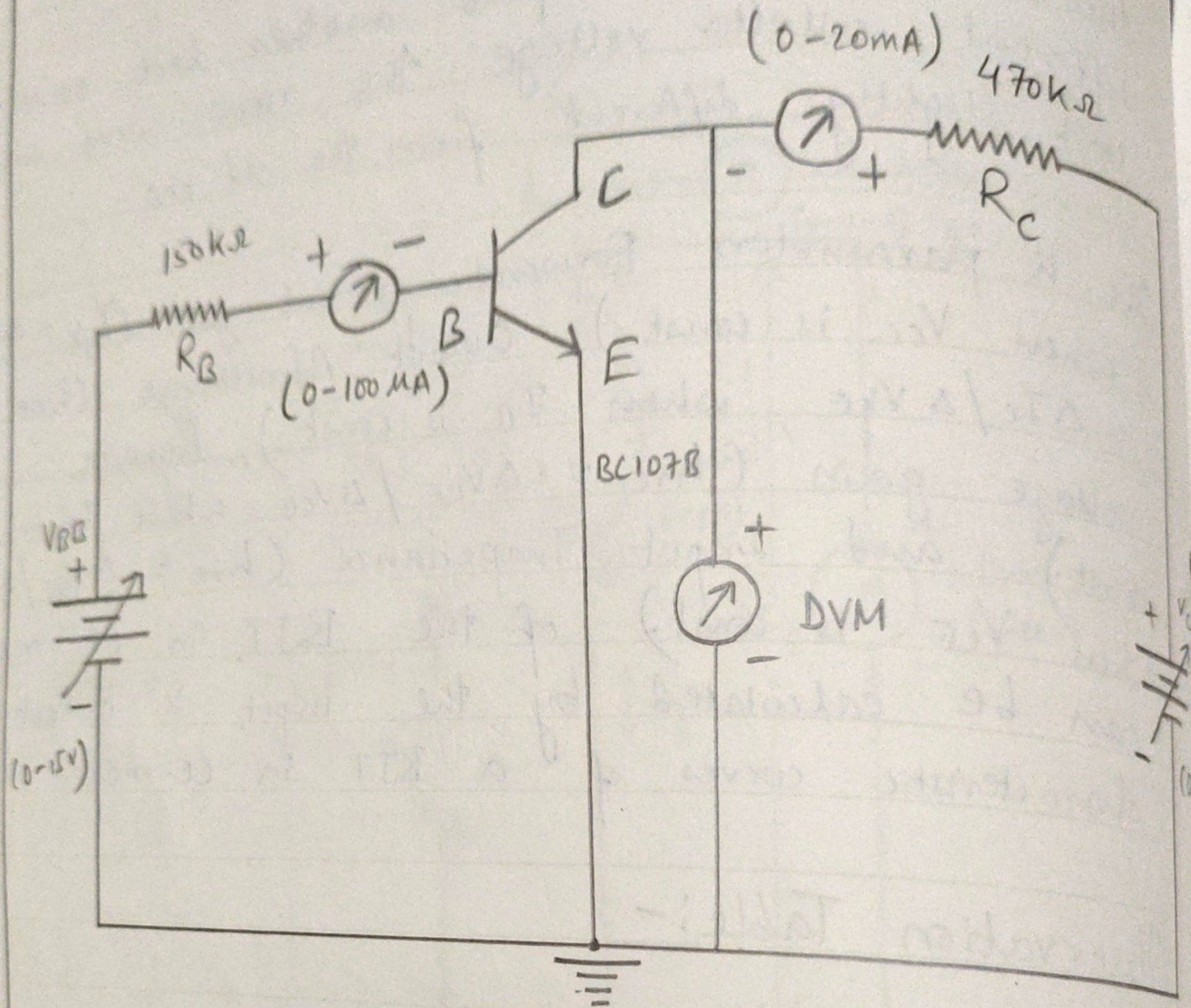
Input characteristic

(Take readings upto 50 μA).

$V_{CE} = 0V$		$V_{CE} = 0V \quad 2V$	
$V_{BE} = (V)$	$I_B (\mu A)$	$V_{BE} (V)$	$I_B (\mu A)$
0	0	0	0
0.1	0	0.1	0
0.2	0	0.2	0
0.3	0	0.3	0
0.4	0	0.4	0

output characteristic

Circuit Diagram:-



DVM:- Digital Volt Meter.

0.5	2	0.5	1
0.55	8	0.55	2
0.6	44	0.6	2
0.62	80	0.62	4
0.64		0.64	7
0.66		0.66	16
0.68		0.68	19

Output characteristics

$I_B = 10 \mu A$		$I_B = 20 \mu A$		$I_B = 30 \mu A$	
V_{CE}	I_C	V_{CE}	I_C	V_{CE}	I_C
(V)	(mA)	(V)	(mA)	(V)	(mA)
0	0	0	0	0	0
0.1	0.83	0.1	2.24	0.1	2.69
0.2	1.81	0.2	4.43	0.2	6.31
0.3	1.97	0.3	4.84	0.3	7.11
0.4	2.02	0.4	4.87	0.4	7.29
0.5	2.03	0.5	4.89	0.5	7.36
0.6	2.03	0.6	4.92	0.6	7.36
1.0	2.04	1.0	4.94	1.0	7.45
1.5	2.05	1.5	4.99	1.5	7.50
2.0	2.06	2.0	5.02	2.0	7.56
2.5	2.07	2.5	5.05	2.5	7.61
3.0	2.08	3.0	5.07	3.0	7.65
3.5	2.09	3.5	5.10	3.5	7.70

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$$

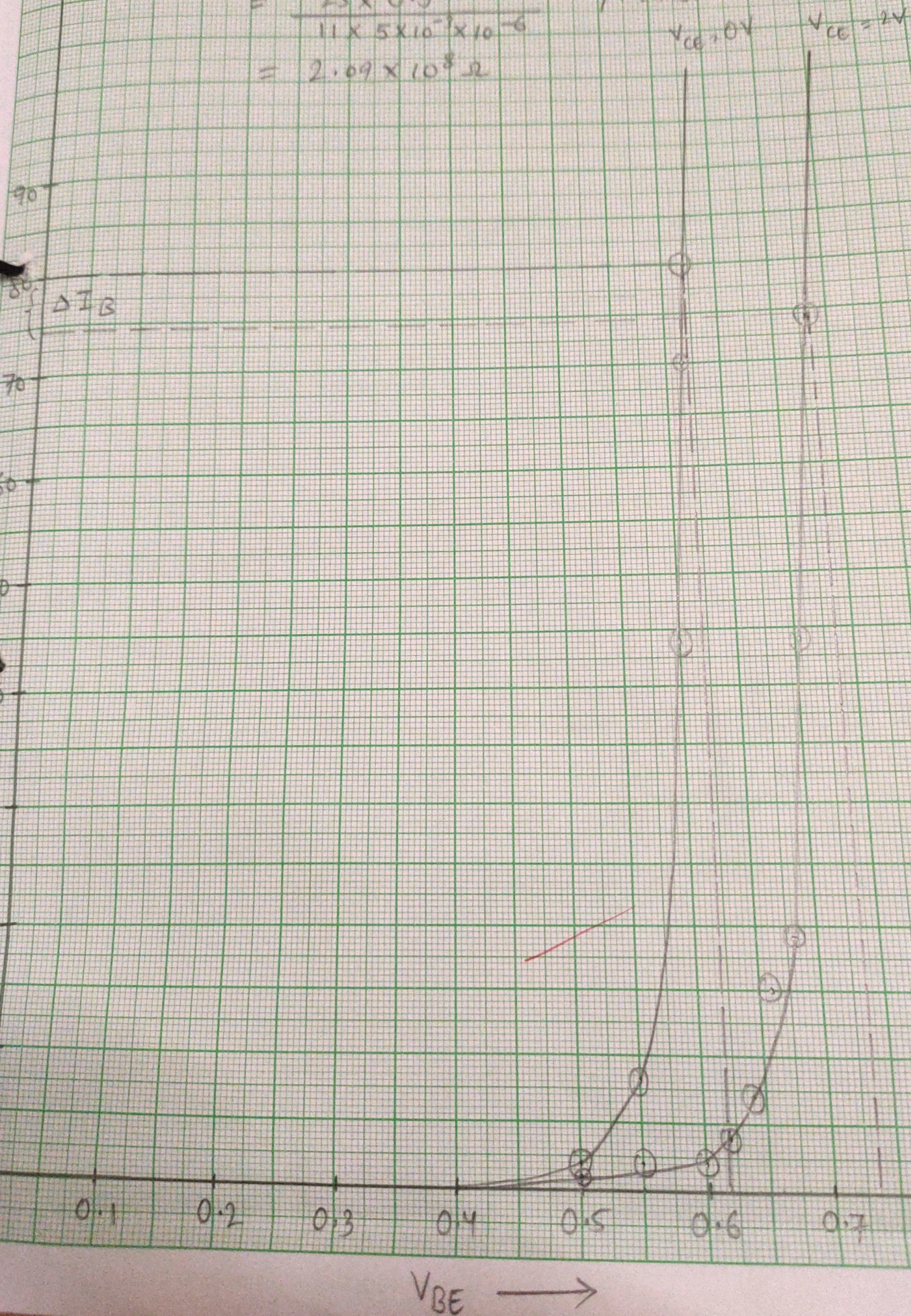
$$= \frac{23 \times 0.5}{11 \times 5 \times 10^{-3} \times 10^{-6}}$$

$$= 2.09 \times 10^8 \Omega$$

Scale :-

1 small box = 5×10^{-3} units along x-axis

1 small box = 0.5 units along y-axis.



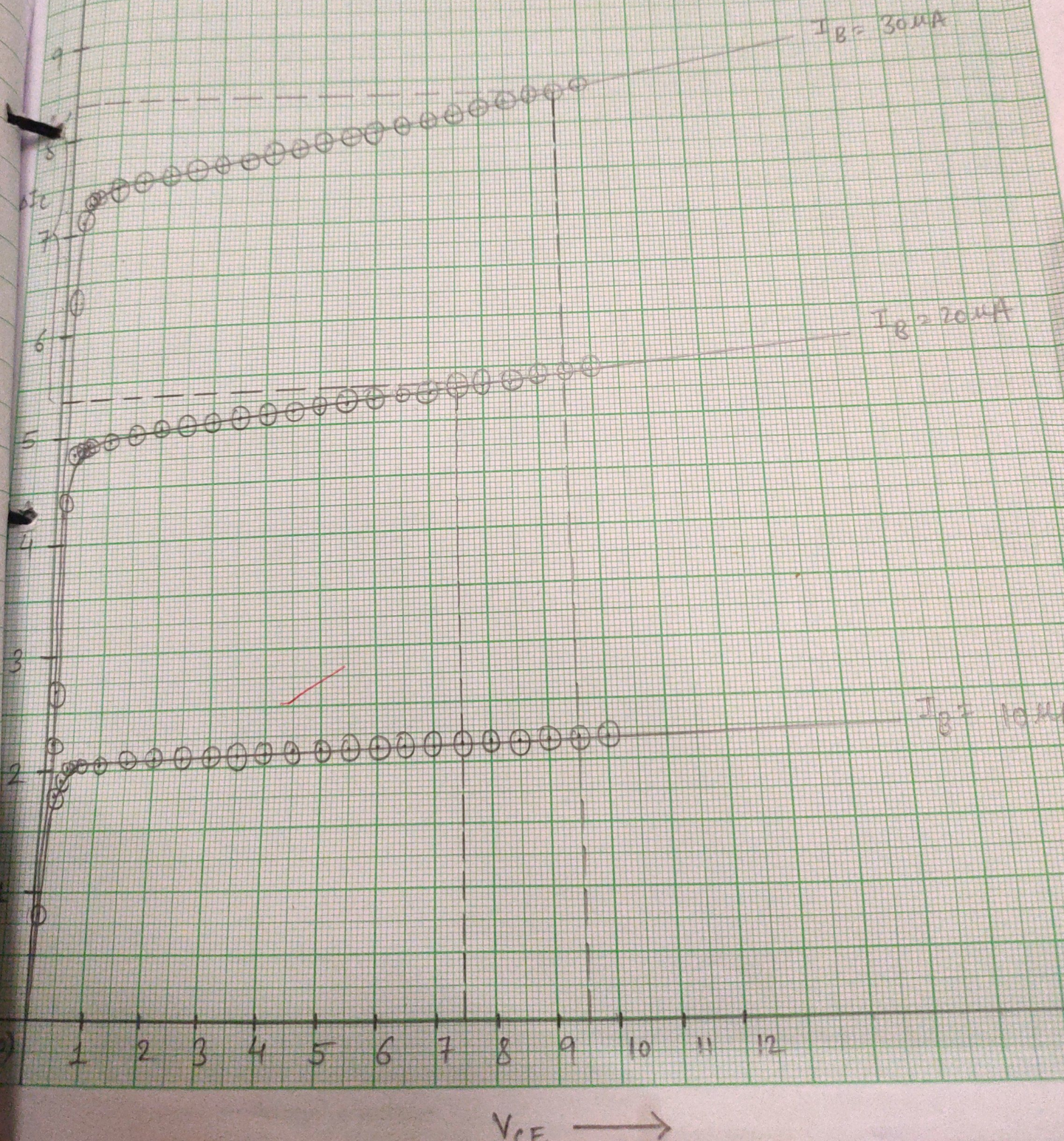
Scale :- 1 small box = 0.1 units along x-axis
 1 small box = 0.05 units along y-axis.

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$$

$$= \frac{60 \times 0.05 \times 10^{-3}}{20 \times 0.1}$$

$$= 0.15 \times 10^{-3} \Omega^{-1}$$

$$= 1.5 \times 10^{-4} \Omega^{-1}$$



4.0	2.1	4.0	5.12	4.0	7.77
4.5	2.11	4.5	5.15	4.5	7.82
5.0	2.12	5.0	5.18	5.0	7.87
5.5	2.12	5.5	5.20	5.5	7.93
6.0	2.13	6.0	5.23	6.0	7.99
6.5	2.14	6.5	5.26	6.5	8.03
7.0	2.14	7.0	5.28	7.0	8.06
7.5	2.15	7.5	5.31	7.5	8.12
8.0	2.16	8.0	5.33	8.0	8.20
8.5	2.17	8.5	5.35	8.5	8.27
9.0	2.17	9.0	5.41	9.0	8.31
9.5	2.18	9.5	5.42	9.5	8.35
10	2.18	10	5.46	10	8.40

Calculations:-

Forward current gain: $h_{fe} = \frac{\Delta I_C}{\Delta I_B}$ when V_{CC} is const.

$$= \frac{60}{11} = 5.45$$

Output admittance:- $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}}$ when I_B is const.

$$= \frac{60 \times 0.05 \times 10^{-3}}{20 \times 0.1}$$

$$= 1.5 \times 10^{-4} \Omega^{-1} \text{ (from graph).}$$

Reverse voltage gain:- $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$ when I_B is const.

$$\Rightarrow \frac{\Delta V_{BE}}{\Delta V_{CE}} = \frac{23}{20} = 1.15$$

Input Impedance :- $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B}$ when V_{CE} is const.

$$= \frac{23 \times 0.5}{11 \times 5 \times 10^{-3} \times 10^{-6}}$$

$$= 2.09 \times 10^8 \Omega$$

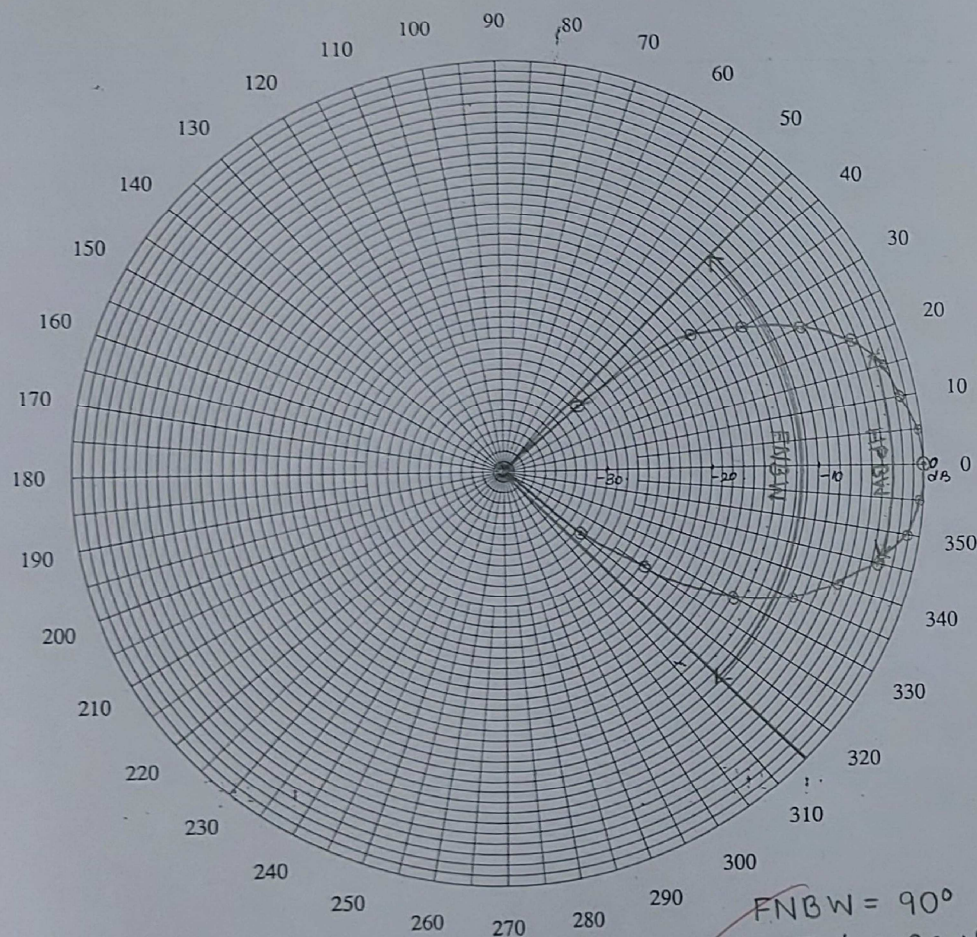
Conclusion:-

In this experiment we have learned that output and input characteristics of a transistor (npn) we know about forward current gain, output admittance, reverse voltage gain and input impedance.

~~16/11/19~~

Name : Komal Kanti Ganguly.

Roll-28. Antenna type :- 3-element Yagi-Uda folded dipole.



$$D = \frac{41000^D}{\theta_{HP} \times \phi_{HP}} = \frac{41000^D}{36.1^\circ \times 36.1^\circ} = 31.46$$

$$\text{or } D = 10 \log_{10} 31.46 = 14.98 \text{ dBi}$$

FNBW = 90°
HPBW = 36.1°

Front-to-back ratio
 $0 - (-40) = -40 \text{ dBi}$

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Page No. _____

Observations :-

S.No	L of rotation (in degree)	Received Signal Amplitude (in uA)	Normalised Signal (B).	$20 \log (B)$ (in dBi).
1	0	31	1	0
2	5	30	0.97	-0.26
3	10	26	0.84	-1.51
4	15	24	0.77	-2.27
5	20	18	0.58	-4.73
6	25	12	0.39	-8.18
7	30	7	0.22	-13.15
8	35	4	0.13	-17.72
9	40	1	0.03	-30.45
10	45	0	0	-40
11	50	"	"	"
12	55	"	"	"
13	60	"	"	"
14	65	"	"	"
15	70	"	"	"
16	75	"	"	"
17	80	"	"	"
18	85	"	"	"
19	90	"	"	"
20	95	"	"	"
21	100	"	"	"
22	105	"	"	"
23	110	"	"	"
24	115	"	"	"

Teacher's Signature : _____

OXFORD

PRACTICAL NOTE BOOK



Botany



Name DIKSHA DEB

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Department of Electronics & Communication Engineering

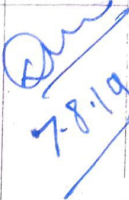
Name of the Paper: Microprocessor & Microcontroller lab

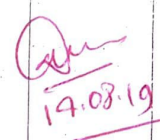
Paper code:

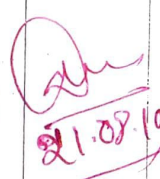
Name of the student: Dikhcha Deb

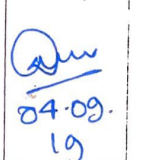
Branch: ECE

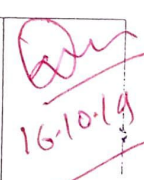
Roll no: 37

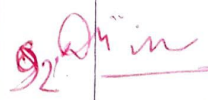
Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)					Marks	Total marks	Signature of teacher with date
P2	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		18	84	 7-8-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		18		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 07/08/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

P3	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		19	85	 14-08-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		18		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 14/08/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

P4	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		20	85	 21-08-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		18		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		17		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 21/08/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

P5	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		20	85	 04-09-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		18		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		17		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 04/09/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

P6	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		22	91	 16-10-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		20		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		19		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 16/10/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

P7	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)		23	92	 24-10-19
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)		20		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)		19		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		
Date: 23/10/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)		10		

Date:	safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)				
	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)				

SILIGURI INSTITUTE OF TECHNOLOGY
Department of Electronics & Communication Engineering

Name of the Paper: <u>Microprocessor and Microcontroller Lab</u>	Paper code:
Name of the student: <u>Diksha Deb</u>	Branch: <u>ECE</u>
	Roll no: <u>11900317037</u>

Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)				Marks	Total marks	Signature of teacher with date
Experiment no: <u>P8</u>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	<u>23</u>	<u>92</u>	<u>Dr</u> <u>06.11.19</u>
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	<u>20</u>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	<u>19</u>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
Date: <u>06/11/19</u>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		

Experiment no: <u>P9</u>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	<u>23</u>	<u>92</u>	<u>Dr</u> <u>15.11.19</u>
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	<u>20</u>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	<u>19</u>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
Date: <u>13/11/19</u>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		

Experiment no: <u>P10</u>	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	<u>22</u>	<u>91</u>	<u>Dr</u> <u>15.11.19</u>
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	<u>20</u>		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	<u>19</u>		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		
Date: <u>15/11/19</u>	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	<u>10</u>		

Experiment no:	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)			
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)			
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)			
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
Date:	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			

Experiment no:	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)			
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)			
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)			
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
Date:	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			

Experiment no:	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)			
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)			
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)			
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
Date:	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			

1. Aim: Addition of 2 eight bit data, data present in internal registers.

Address	Mnemonics	Hexcode	Comments
8000	MVI A, (02) _H	3E	Load 8-bit data in accumulator
8001		02	
8002	MVI B, (04) _H	06	Load 8bit data in a register
8003		04	
8004	ADD B	80	Add the contents of a register to the contents of accumulator
8005	RST3	DF	Stop processing

Output stored in register A = 06_H

2. Aim: Subtraction of 2 eight bit data, data present in internal registers

Address	Mnemonics	Hexcode	Comments
8006	MVI A, (04) _H	3E	Load 8-bit data in accumulator
8007		04	
8008	MVI B, (02) _H	06	Load 8bit data in a register
8009		02	
800A	SUB B	90	Sub the contents of a register from the contents of accumulator
800B	RST3	DF	Stop processing

Output stored in register A = 02_H

3. Aim: Addition of 2 8-bit data after storing it to 2 consecutive memory location and store the output in the next location

Address	Mnemonics	Hex code	Comments
800C	LXI H, (9005) _H	21	Load 16 bit number in register pair
800D		05	
800E		90	
800F	MOV A,M	7E	Copy data from source register to destination register
8010	INX H	23	Increment the content of a register pair
8011	ADD M	86	Add the contents of memory to A
8012	INX H	23	Increment the contents of register pair
8013	MOV M,A	77	Copy the data byte from the register A into memory specified by the address in HL register.
8014	RST3	DF	Stop processing

Input stored in memory 9005 = 02_H
Input stored in memory 9006 = 05_H
Output stored in memory 9007 = 07_H

4. Aim: To add contents of accumulator and memory and keep the result in register.

Address	Mnemonics	Hexcode	Comments
8015	LXI H, (9008) _H	21	Load 16 bit number
8016		08	in register pair
8017		90	
8018	MVI C, (04) _H	0E	Load 8-bit data in
8019		04	register
801A	MOV A, M	7E	Copy the data byte in register A from memory specified by the address in HL register
801B	ADD C	81	Add the contents of register to the contents of accumulator
801C	MOV B, A	47	Copy data from source register to destination register
801D	RST 3	DF	Stop processing

Input stored in memory 9008 = 02_H

Output stored in register B = 06_H

(Handwritten signature)
17.8.19

1

Experiment No.-1

• AIM:- To study pulse amplitude modulation (PAM) and demodulation.

• OBJECTIVE:- ① To study the distortion factor of reconstructed signal as a function of sampling frequency.

② To study the comparison between different order low-pass filter (demodulator).

③ To study the effect of sample and hold circuit.

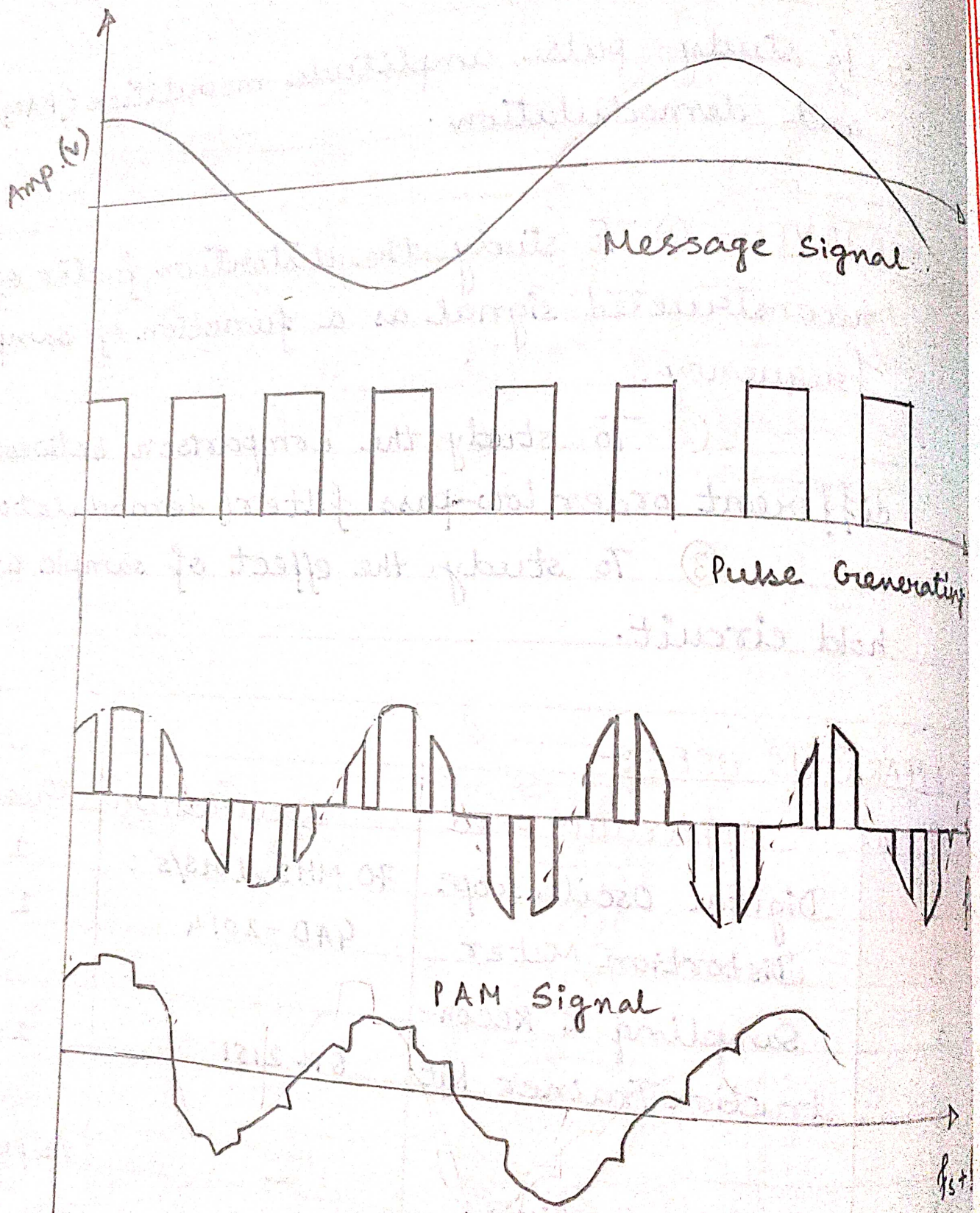
• APPARATUS USED:-

Sl. No.	Apparatus used	Specification	Quantity
1	Digital Oscilloscope	70 MHz, 1Gs/s	1
2	Distortion Meter	GAD-2014	1
3	Sampling & Reconstruction Trainer Kit	ST-2151	1
4.	Connecting Wires.	—	As per require

• TABLE:-

p. T.O.

Teacher's Signature



- THEORY :- Pulse amplitude modulation is a scheme which alters the amplitude of regularly spaced rectangular pulses.

In accordance with the instantaneous values of a continuous message signal. The amplitude of the modulated Pulse represents the amplitude of the intelligence.

A very short pulses of constant amplitude and fast representation rate is chosen the amplitude of these pulse is made to vary in accordance with the of multiplying the short pulses height corresponds to the modulating wave.

The demodulated PAM waves, the signal is passed through low-pass-filter having a cut-off frequency equal to the highest frequency in the modulating signal along with DC component.

PAM has the same signal-to-noise ratio as AM and so it is not employed in the practical circuits.

• OBSERVATION TABLE :-

$$f_m = 1 \text{ KHz},$$

$$V_m = 6 \text{ V}.$$

Table 1 :-

Sampling frequency f_s (KHz)	% Distortion of demodulated signal from 2 nd order filter	% Distortion of demodulated signal from 4 th order filter.
2	62	40
5	41	32
8	18	4
10	11	1.5
20	2.5	0.68
40	0.84	0.6

Table 2 :-

Duty Cycle	Amplitude of Re- constructed signal for natural PAM (V.)	Amplitude of de- constructed signal for S.& Hold Circuit
10	0.7 V	6.8 V
20	1.4 V	6.8 V
30	2.0 V	6.8 V
40	2.7 V	6.8 V
50	3.4 V	6.8 V
60	4 V	6.8 V
70	4.7 V	6.8 V
80	5.3 V	6.8 V
90	6 V	6.8 V

- CONCLUSION:- From this experiment, we come to know that amplitude of reconstructed signal do not depend upon duty cycle. We observed the values of % of distorted signals from 2nd and 4th order filter. We also calculate the values of the amplitudes of re-constructed and de-constructed signals for natural PAM & Sample-Hold Circuits respectively in accordance to duty cycle.

28/02/19

Orion
It's always your choice.



LABORATORY Notebook

Name SUBHAM GHOSH
Class Sec. A Roll No. 19
Subject DSP Year



Paper code: EC 692

Branch: ECE

Roll no: 11900316019

S (b)	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	23	86
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	23	
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8	
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	16	
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8	
04-19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8	

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Name of the Paper:	Paper code:
Name of the student:	Roll no:

Experiment Name/No.	Objective/Criteria	Quality/Score (total evaluation marks = 100)				Marks	Total marks	Signature of teacher with date
Experiment no: 7(a)	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	22	85	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	22		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	17		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
Date: 23/04/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		

Experiment no: 7(b)	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	22	87	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	23		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
Date: 23/04/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		

Experiment no: 7(c)	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	23	90	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	23		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	12		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	9		
Date: 30/04/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	9		

Experiment no: 8	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)	23	91	
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)	23		
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	8		
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)	18		
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	9		
Date: 7/05/19	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)	10		

Experiment no:	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)			
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)			
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)			
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
Date:	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			

Experiment no:	Theoretical concept (25)	Excellent(25-20)	Good(19-14)	Fair(13-7)	Poor(6-0)			
	Experiment conduct(25)	Excellent(25-20)	Good(19-14)	Fair(13-6)	Poor(5-0)			
	Team work(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
	Lab report(20)	Excellent(20-15)	Good(14-10)	Fair(9-6)	Poor(5-0)			
	Experimental setup & safety (10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			
Date:	Discipline(10)	Excellent(10-8)	Good(7-6)	Fair(5-4)	Poor(3-0)			

EXPERIMENT NO: 3

Aim: To obtain the output sequence $y(n)$ using Convolution Sum.

Theory: Convolution is a mathematical operation used to express the relation between input and output of an LTI system. If we define $y(n)$ as the convolution of signals $x(n)$ and $h[n]$, then we write

$$y(n) = \sum_{k=-\infty}^{\infty} h(k) x[n-k]$$

A systematic, detailed procedure for evaluating this sum is given in Graphical Evaluation of Discrete Time Convolution. In brief we first form a signal $v_n[k] = h[k]x[n-k]$ for a desired value of n , to obtain $y[n]$. We graph $h[k]$ and graph $x[n-k]$ as a function of the independent variable k . In order to graph $x[n-k]$, first reflex $x[k]$ about $k=0$ to obtain $x[-k]$ then shift $x[-k]$ right by n values to obtain $x[n-k]$. It is usually quite simple to identify the product $v_n[k] = h[k]x[n-k]$ from the graph of $h[k]$ and $x[n-k]$. The process is repeated for all values n , where $y[n]$ is desired.

MATLAB PROGRAM:-

```
disp('PROGRAM TO PERFORM LINEAR CONVOLUTION')
```

```
disp('Generation of sequence x(n)')
```

```
x = [1 2 3 4];
```

```
nmin = 0;
```


$T_s = 1;$

$n_1 = n_{min1} : T_s : n_{min1} + \text{length}(x) - 1;$

`subplot(3,1,1);`

`stem(n1,x);`

`xlabel('n');`

`ylabel('x(n)');`

`title('Input sequence');`

`disp('Generation of the sequence h(n)')`

$h = [4 \ 3 \ 2 \ 1];$

$n_{min2} = -1;$

$n_2 = n_{min2} : T_s : n_{min2} + \text{length}(h) - 1$

`subplot(3,1,2);`

`stem(n2,h);`

`xlabel('n');`

`ylabel('h(n)');`

`title('Impulse Response')`

`disp('Generation of the convolved sequence y(n)')`

$y = \text{conv}(x,h)$

$n_{min} = \min(n_{min1}, n_{min2});$

$y_{len} = \text{length}(x) + \text{length}(h) - 1;$

$n_{max} = n_{min} + y_{len} - 1;$

$n = n_{min} : T_s : n_{max};$

`subplot(3,1,3);`

`stem(n,y)`

`xlabel('n')`

$$x(n) = \{1, 2, 3, 4\}$$



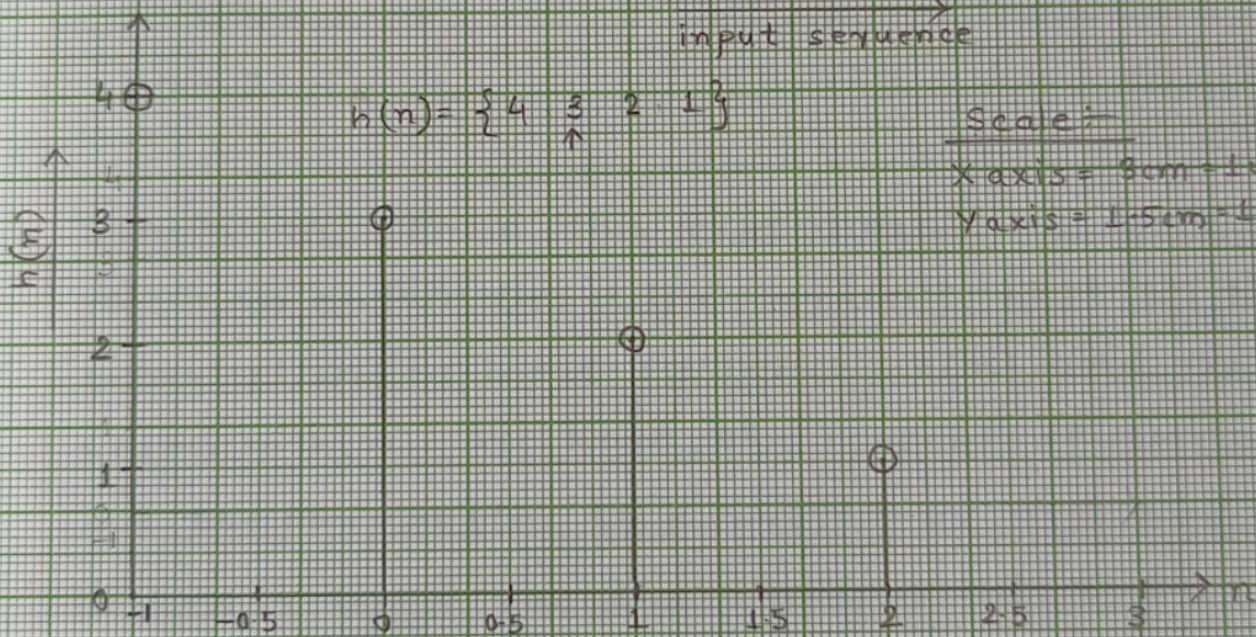
Scale

X axis = 3cm = 1 unit

Y axis = 1.5cm = 1 unit

input sequence

$$h(n) = \{4, 3, 2, 1\}$$



Scale:

X axis = 3cm = 1 unit

Y axis = 1.5cm = 1 unit

impulse response



Scale

X axis = 2cm = 1 unit

Y axis = 2cm = 1 unit

$$y(n) = \{2, 10, 20, 30, 20, 10, 2\}$$

output sequence

`ylabel('y(n)');`

`title('Output sequence')`

OUTPUT VALUES:-

Taken,

$$x = [1 \ 2 \ 3 \ 4]$$

$$n_{min1} = 0$$

$$h = [4 \ 3 \ 2 \ 1]$$

$$n_{min2} = -1$$

Conclusion:- From this experiment we conclude that we can obtain the output sequence just by doing the convolution of input sequence $x(n)$ and impulse response $h(n)$. We have the concept of convolution and the properties of convolution and how the discrete signal can be represented as the unweighted sum of the unit impulse signal.

✓
29/3/19



THURS

TUES DAY

Attendance Register for

the

Sl.

ECE 6th sem 2019		GR-A
SL	ROLL	NAME
1	11900316009	YASH VARDHAN
2	11900316010	UTSA GHOSH
3	11900316011	TRIDIBESH NAYEK
4	11900316012	TANMOY DEY
5	11900316013	TANIYA CHATTERJEE
6	11900316014	SUSMITA CHOWDHURY
7	11900316015	SUSHMITA SARKAR
8	11900316016	SUPRATIV SENGUPTA
9	11900316017	SUDESHNA SAHA
10	11900316018	SUBHAM UPADHYAY
11	11900316019	SUBHAM GHOSH
12	11900316020	SOUVIK MONDAL
13	11900316021	SOUMYADEEP PAUL
14	11900316022	SHIVAM SINHA
15	11900316023	SHAYATA SARKAR
16	11900316024	SHANKHADEEP DEY
17	11900316025	SEJUTI ROY MUKHERJEE
18	11900316026	SAYANTANI DEY
19	11900316027	SAYANI MAITRA
20	11900316028	SAURAV KUMAR VERMA
21	11900316029	SANDIPAN BHATTACHARJEE
22	11900316030	SANDEEP DAS
23	11900316031	SAGNIK KUMAR SINHA
24	11900316032	RUPESH RAJ
25	11900316034	RISHAV KUMAR MAHATO

A1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
09	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
10	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
11	P	.	(P)	.	.	.	.	.	.	.	.	.	.	.	.	.	.
12	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
13	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
14	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
15	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16	P	.	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
17	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
18	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
19	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
20	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
21	.	.	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
22	.	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
23	.	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
24	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
25	P	.	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
26	P	.	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
27	.	(P)	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
28	P	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
29	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
30	.	(P)	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
31	.	P	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.
32	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
34	P	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.

LAB 1. unit impulse, step, ramp, exponential

LAB 2. & rest sine, cosine

LAB 3. linear convolution

LAB 4. Impulse Response & Step Response.

Z-Transform & Pole-Zero

DFT & IDFT (Take $F(a)$ & $F(b)$)Circular Convolution $F(a)$

IIR Butterworth filter using Impulse invariance.

